PRELIMINARY DATA SHEET

NEC

# MOS INTEGRATED CIRCUIT

# μPD65949S1-P00-F6

## BONITO™ - Companion Chip for VR43xx and VR5xxx

### DESCRIPTION

'Bonito' is a system controller especially designed for MIPS® RISC microprocessors with a 32-bit SysAD bus. 'Bonito' incorporates a simple and fast memory interface for PC-100 compliant SDRAMs, a Rev 2.1 compliant 33 MHz/32-bit PCI interface and last but not least a 16-bit local bus with IDE support. It has a built-in, flexible interrupt controller and numerous general purpose I/Os. In applications using the 32-bit SysAD bus (e.g. VR43xx, VR5432 and VR5500 based systems) it reduces the number of required parts significantly. 'Bonito' comes in a compact 352-pin plastic BGA package.

'Bonito' is designed as system controller for MIPS® RISC CPU based systems. The combination of 'Bonito' with a MIPS® RISC microprocessor gives you an excellent performance/cost ratio for computing or data traffic intensive applications like high resolution printers, scanners, networking equipment, high end Set-Top-Boxes or PC-Peripherals.

**Functions in detail are described in Bonito's specification.**
**The latest version of this specification can be downloaded from Algorithmics' website:**

**www.algor.co.uk**

**Be sure to read this specification when you design your systems.**

### FEATURES

- Direct connection to any MIPS R4x00 CPU with a 32-bit SysAD bus
- Direct connection to 32-bit 33 MHz PCI bus, conforming to Rev. 2.1
- Integrated PCI arbiter acting as PCI master or target
- Independent CPU and PCI input clocks
- Internal 'cache' for local memory locations provides greatly enhanced PCI transfer performance for device controllers which are PCI bus initiators
- PCI/local-memory copier for applications requiring bulk data transport
- 16-bit local I/O bus for local ROM and 'slow' peripherals
- High performance SDRAM memory interface using standard PC-100 parts in either 32- or 64-bit arrays, including 100-, 144- or 168- pin DIMMs
- DMA support for faster devices on the local I/O bus, including 'UDMA' transfers as defined in the ATA-4 standard for PC disk drives
- Configurable debug mode
- Glueless support of CPU reset sequence
- Includes useful generic interrupt controller
- Configurable from ROM, pins or PCI bus
- Supports all VR43xx, VR5432 and VR5500 bus modes
- Operating voltage: 3.3 V, 5 V tolerant I/O
- Compact 352-pin 1.27 mm pitch BGA package

### ORDERING INFORMATION

| Device | Part Number | Package | Operating Frequency |
|---|---|---|---|
| Bonito | μPD65949S1-P00-F6 | 352 P-BGA | 91 MHz |

**The information contained in this document is released in advance of the production cycle for the device. The parameters for the device may change before final production, or NEC Corporation may, at its own discretion, withdraw the device prior to production.**



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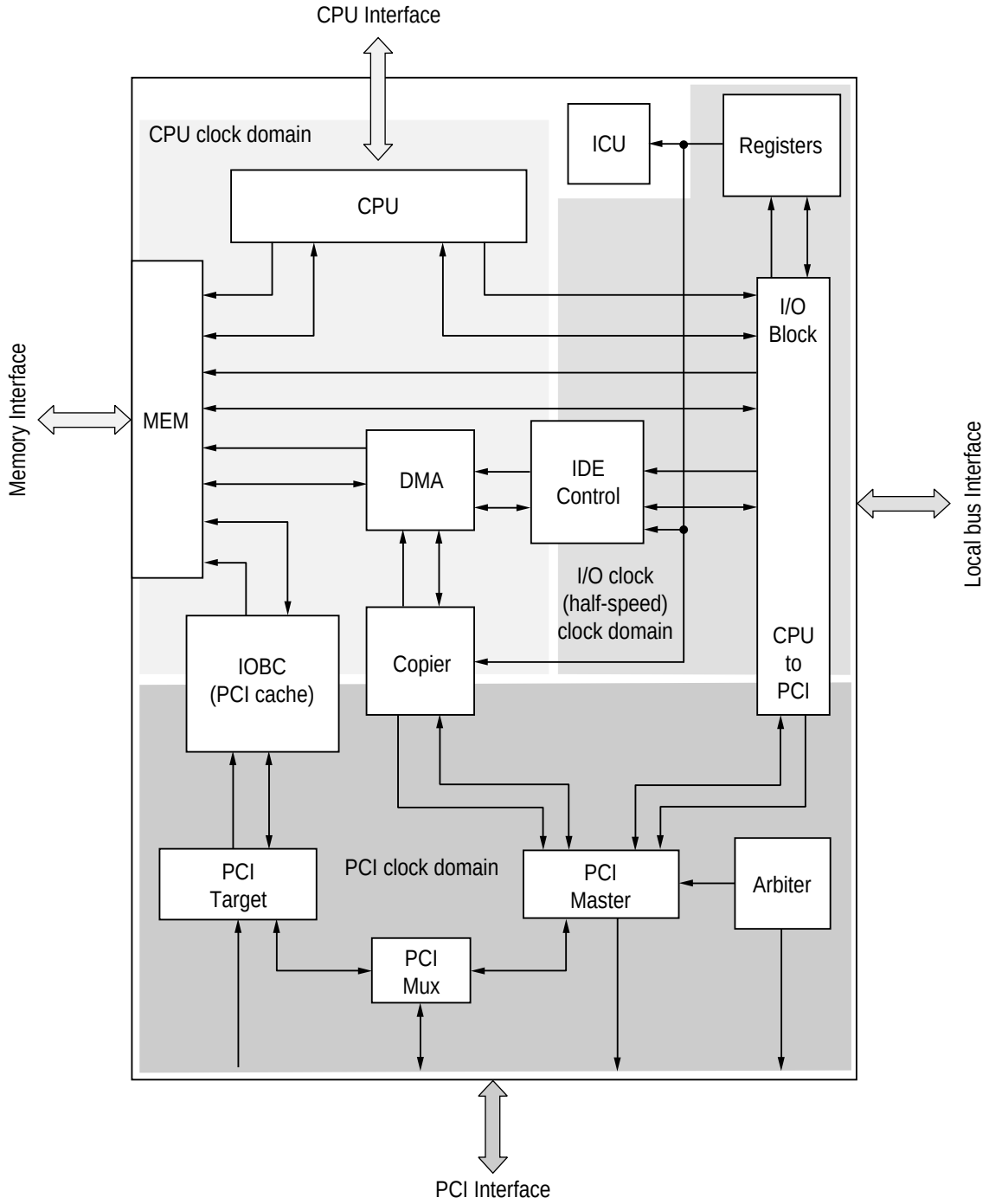
## INTERNAL BLOCK DIAGRAM

***Figure In-1: Internal Block Diagram***




**Remark:** The line with two arrows shows data flow.
The line with only one arrow shows control flow.

## PIN IDENTIFICATION

| | |
|---|---|
| AD(31:0) | PCI address/data |
| $\overline{\text{CBE(3:0)}}$ | PCI command/byte enable |
| CLK | PCI clock |
| ClockIn | Clock buffer input |
| ClockOut(5:0) | Clock buffer output |
| CPUClock | Clock input |
| $\overline{\text{CPUColdReset}}$ | CPU cold reset output |
| $\overline{\text{CPUReset}}$ | CPU reset output |
| DBA(1:0) | SDRAM bank select |
| $\overline{\text{DCAS}}$ | SDRAM $\overline{\text{CAS}}$ output |
| DCKE | SDRAM clock enable |
| $\overline{\text{DCS(1:0)H}}$ | SDRAM chip select |
| $\overline{\text{DCS(1:0)L}}$ | SDRAM chip select |
| DD(31:0) | SDRAM data |
| $\overline{\text{DMACK}}$ | DMA acknowledge |
| DMARQ | DMA request |
| DDMuxLo | SDRAM multiplexer control |
| DDMuxHi | SDRAM multiplexer control |
| DDP(3:0) | SDRAM data parity |
| DEVSEL | PCI device select |
| DQMBLo/Hi | SDRAM byte enable |
| $\overline{\text{DRAS}}$ | SDRAM RAS output |
| $\overline{\text{DWE}}$ | SDRAM write enable |
| EOK | SysAD bus control |
| $\overline{\text{EValid}}/\overline{\text{ValidIn}}$ | SysAD bus control |
| $\overline{\text{FRAME}}$ | PCI cycle control |
| GND | Ground |
| $\overline{\text{GNT(5:0)}}$ | PCI bus grant |
| GPIn(5:0) | General purpose input |
| GPIO(8:0) | General purpose I/O port |
| IDSEL | PCI cycle control |
| Int(1:0) | Interrupt Output |
| IOA(4:0) | I/O bus address |
| IOCS(3:0) | I/O bus chip select |
| IOD(15:0) | I/O bus data |
| $\overline{\text{IODEN}}$ | I/O bus data buffer enable |
| IODIR | I/O bus data direction control |
| $\overline{\text{IORd}}$ | I/O bus read strobe |
| IORDY | I/O channel ready |
| $\overline{\text{IOWr}}$ | I/O bus write strobe |
| $\overline{\text{IRDY}}$ | PCI cycle control |
| $\overline{\text{IRQA}}$ | PCI interrupt request |
| Isolate | I/O bus isolation from SDRAM |
| JTCK | JTAG clock |
| JTDI | JTAG data input |
| JTDO | JTAG data output |
| JTMS | JTAG mode select |
| $\overline{\text{LOCK}}$ | PCI bus lock |
| ModeClock | Mode configuration clock input |
| ModeIn | Mode data output |
| Mux(13:0) | SDRAM address |
| PAR | PCI parity |
| $\overline{\text{PERR}}$ | PCI parity error |
| $\overline{\text{PMaster}}$/Release | SysAD bus control |
| $\overline{\text{PValid}}/\overline{\text{ValidOut}}$ | SysAD bus control |
| $\overline{\text{REQ(5:0)}}$ | PCI bus request |
| $\overline{\text{RESET}}$ | PCI Reset |
| $\overline{\text{ROMCS(1:0)}}$ | ROM chip select |
| $\overline{\text{SERR}}$ | PCI system error |
| $\overline{\text{STOP}}$ | PCI cycle control |
| SysAD(31:0) | SysAD bus address/data |
| SysADC(3:0) | SysAD bus parity |
| SysCmd(8:0) | SysAD bus command lines |
| $\overline{\text{SysController}}$ | Reset control configuration |
| $\overline{\text{SysReset}}$ | Reset input |
| $\overline{\text{TRDY}}$ | PCI cycle control |
| VCCOk | CPU control output |
| $V_{D5}$ | PCI power supply |
| $V_{DD}$ | Power supply |

## PIN CONFIGURATION

- 352-Pin Plastic BGA (35 x 35 mm) (Top View)

***Figure In-2: Pin Configuration***

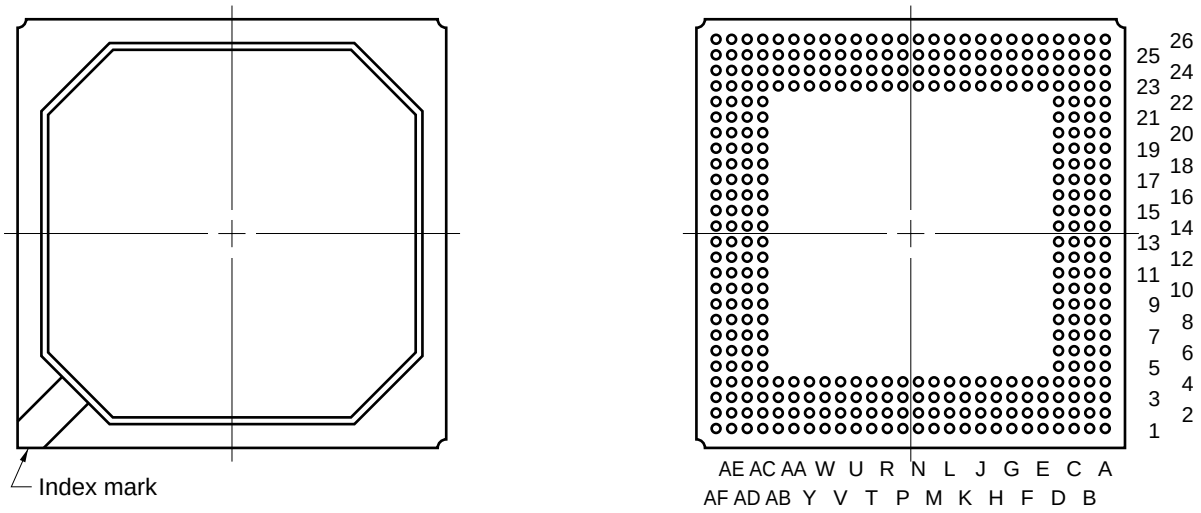



***Table In-1: Pin Configuration (1/3)***

| Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name |
|---|---|---|---|---|---|---|---|
| A1 | GND | A23 | IOD14 | B19 | IOD2 | U17 | AD7 |
| A2 | GND | A24 | IOD15 | B2 | IOD5 | U18 | AD3 |
| A3 | CLK | A25 | GPIO0 | B21 | IOD8 | U19 | AD1 |
| A4 | $V_{DD}$ | A26 | GND | B22 | IOD11 | U20 | $V_{D5}$ |
| A5 | $V_{D5}$ | B1 | $\overline{CBE3}$ | B23 | GPIO1 | V1 | IOD1 |
| A6 | AD19 | B2 | GND | B24 | GPIO2 | V2 | $V_{DD}$ |
| A7 | AD16 | B3 | GND | B25 | GND | V3 | IOD7 |
| A8 | $\overline{TRDY}$ | B4 | AD23 | B26 | GND | V4 | IOD10 |
| A9 | $\overline{DEVSEL}$ | B5 | AD20 | C1 | AD24 | V5 | IOD13 |
| A10 | $\overline{PERR}$ | B6 | AD18 | C2 | $V_{D5}$ | V6 | GND |
| A11 | $\overline{CBE1}$ | B7 | $\overline{CBE2}$ | C3 | GND | V7 | GPIO3 |
| A12 | GND | B8 | GND | C4 | AD22 | V8 | GPIO4 |
| A13 | AD11 | B9 | $\overline{STOP}$ | C5 | AD21 | V9 | AD26 |
| A14 | GND | B10 | $\overline{SERR}$ | C6 | AD17 | V10 | AD25 |
| A15 | VD5 | B11 | AD15 | C7 | $\overline{FRAME}$ | V11 | GND |
| A16 | AD5 | B12 | AD14 | C8 | $V_{DD}$ | V12 | GND |
| A17 | AD2 | B13 | AD10 | C9 | $V_{D5}$ | V13 | GND |
| A18 | GND | B14 | $V_{DD}$ | C10 | PAR | V14 | $V_{DD}$ |
| A19 | IOD3 | B15 | $\overline{CBE0}$ | C11 | $V_{DD}$ | V15 | $\overline{IRDY}$ |
| A20 | IOD6 | B16 | AD4 | C12 | AD13 | V16 | GND |

***Table In-1: Pin Configuration (2/3)***

| Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name |
|---|---|---|---|---|---|---|---|
| A21 | IOD9 | B17 | $V_{DD}$ | C13 | AD9 | V17 | GND |
| A22 | IOD12 | B18 | IOD0 | C14 | $V_{D5}$ | V18 | $V_{D5}$ |
| D11 | $V_{DD}$ | J1 | $\overline{GNT1}$ | R1 | MUX11 | AA1 | DQMBLo |
| D12 | AD12 | J2 | $V_{DD}$ | R2 | MUX10 | AA2 | DBA0 |
| D13 | AD8 | J3 | $\overline{GNT0}$ | R3 | MUX9 | AA3 | $\overline{DDMuxLo}$ |
| D14 | GND | J4 | $\overline{REQ5}$ | R4 | MUX8 | AA4 | $V_{DD}$ |
| D15 | AD6 | J23 | GND | R23 | GND | AA23 | $V_{DD}$ |
| D16 | $V_{DD}$ | J24 | JTDI | R24 | ClockOut4 | AA24 | $\overline{INT1}$ |
| D17 | GND | J25 | $\overline{IOCS1}$ | R25 | ClockIn | AA25 | SysCmd2 |
| D18 | AD0 | J26 | IODIR | R26 | $V_{DD}$ | AA26 | $\overline{PMaster}$ |
| D19 | GND | K1 | $\overline{GNT3}$ | T1 | MUX7 | AB1 | $\overline{DCAS}$ |
| D20 | IOD24 | K2 | GND | T2 | MUX6 | AB2 | DCKE |
| D21 | $V_{DD}$ | K3 | $\overline{GNT2}$ | T3 | MUX5 | AB3 | $\overline{DDMuxHi}$ |
| D22 | GND | K4 | GND | T4 | $V_{DD}$ | AB4 | $V_{DD}$ |
| D23 | GND | K23 | GND | T23 | $V_{DD}$ | AB23 | SysADC1 |
| D24 | GPIO5 | K24 | $\overline{IODEN}$ | T24 | ClockOut5 | AB24 | SysCmd6 |
| D25 | GPIn0 | K25 | $\overline{ROMCS1}$ | T25 | DMARQ | AB25 | SysCmd1 |
| D26 | GPIO6 | K26 | $\overline{IOCS2}$ | T26 | ModeClock | AB26 | SysCmd0 |
| E1 | AD29 | L1 | $\overline{GNT5}$ | U1 | MUX4 | AC1 | DD31 |
| E2 | AD28 | L2 | $V_{D5}$ | U2 | GND | AC2 | GND |
| E3 | AD27 | L3 | $\overline{GNT4}$ | U3 | MUX3 | AC3 | DD27 |
| E4 | $V_{D5}$ | L4 | $V_{DD}$ | U4 | MUX2 | AC4 | GND |
| E23 | GPIn1 | L23 | $V_{DD}$ | U23 | IORDY | AC5 | DD21 |
| E24 | GPIO7 | L24 | $\overline{IOCS3}$ | U24 | $\overline{SysController}$ | AC6 | $V_{DD}$ |
| E25 | GPIn2 | L25 | $\overline{IORD}$ | U25 | ModeIn | AC7 | DD14 |
| E26 | GPIn3 | L26 | $\overline{ROMCS0}$ | U26 | TEST1 | AC8 | GND |
| F1 | AD31 | M1 | $\overline{IRQA}$ | V1 | $\overline{DCS0H}$ | AC9 | DD7 |
| F2 | AD30 | M2 | $\overline{RESET}$ | V2 | MUX1 | AC10 | DD3 |
| F3 | $V_{DD}$ | M3 | $\overline{LOCK}$ | V3 | $\overline{DCS1H}$ | AC11 | $V_{DD}$ |
| F4 | $V_{DD}$ | M4 | $V_{DD}$ | V4 | GND | AC12 | GND |
| F23 | $V_{DD}$ | M23 | IOA1 | V23 | TEST2 | AC13 | GND |
| F24 | GPIO8 | M24 | $\overline{DMACK}$ | V24 | TEST0 | AC14 | SysAD27 |
| F25 | JTCK | M25 | IAO0 | V25 | $\overline{EValid}$ | AC15 | SysAD23 |
| F26 | SMC | M26 | $\overline{IOWR}$ | V26 | VCCOk | AC16 | $V_{DD}$ |
| G1 | $\overline{REQ2}$ | N1 | n.c. | W1 | $\overline{DCS0L}$ | AC17 | SysAD16 |
| G2 | $\overline{REQ1}$ | N2 | $V_{D5}$ | W2 | $\overline{DCS1L}$ | AC18 | GND |
| G3 | $\overline{REQ0}$ | N3 | MUX13 | W3 | DBA1 | AC19 | SysAD10 |
| G4 | GND | N4 | GND | W4 | MUX0 | AC20 | SysAD6 |
| G23 | GPIn4 | N23 | ClockOut1 | W23 | GND | AC21 | $V_{DD}$ |

*Table In-1: Pin Configuration (3/3)*

| Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name | Pin Number | Pin Name |
|---|---|---|---|---|---|---|---|
| G24 | GPIn5 | N24 | IOA3 | W24 | $\overline{\text{CPUReset}}$ | AC22 | GND |
| G25 | JTRST | N25 | ClockOut0 | W25 | $\overline{\text{EOK}}$ | AC23 | GND |
| G26 | $V_{DD}$ | N26 | IOA2 | W26 | $\overline{\text{CPUColdReset}}$ | AC24 | SysCmd5 |
| H1 | $\overline{\text{REQ4}}$ | P1 | do not connect. | Y1 | $V_{DD}$ | AC25 | TMD2 |
| H2 | $V_{D5}$ | P2 | IDSEL | Y2 | $\overline{\text{DWE}}$ | AC26 | GND |
| H3 | $\overline{\text{REQ3}}$ | P3 | MUX12 | Y3 | DQMBHi | AD1 | DD30 |
| H4 | GND | P4 | $V_{D5}$ | Y4 | $\overline{\text{DRAS}}$ | AD2 | DD29 |
| H23 | $\overline{\text{IOCS0}}$ | P23 | GND | Y23 | $\overline{\text{INT0}}$ | AD3 | GND |
| H24 | JTMS | P24 | IOA4 | Y24 | $\overline{\text{SYSReset}}$ | AD4 | DD24 |
| H25 | Isolate | P25 | ClockOut3 | Y25 | $V_{DD}$ | AD5 | DD20 |
| H26 | JTDO | P26 | ClockOut2 | Y26 | $\overline{\text{PValid}}$ | AD6 | DD17 |
| AD7 | DD13 | AD25 | CPUClk | AE17 | GND | AF9 | DD4 |
| AD8 | DD10 | AD26 | TMD1 | AE18 | SysAD12 | AF10 | DD0 |
| AD9 | DD6 | AE1 | GND | AE19 | SysAD8 | AF11 | DDP2 |
| AD10 | DD2 | AE2 | GND | AE20 | SysAD4 | AF12 | DDP0 |
| AD11 | $V_{DD}$ | AE3 | DD26 | AE21 | SysAD2 | AF13 | SysAD28 |
| AD12 | SysAD31 | AE4 | DD23 | AE22 | SysADC3 | AF14 | SysAD24 |
| AD13 | SysAD30 | AE5 | DD19 | AE23 | SysCmd8 | AF15 | SysAD20 |
| AD14 | SysAD26 | AE6 | DD16 | AE24 | SysCmd4 | AF16 | SysAD17 |
| AD15 | SysAD22 | AE7 | DD12 | AE25 | GND | AF17 | SysAD14 |
| AD16 | SysAD19 | AE8 | DD9 | AE26 | TMD0 | AF18 | SysAD11 |
| AD17 | SysAD15 | AE9 | DD5 | AF1 | GND | AF19 | SysAD7 |
| AD18 | SysAD13 | AE10 | DD1 | AF2 | DD28 | AF20 | $V_{DD}$ |
| AD19 | SysAD9 | AE11 | DDP3 | AF3 | DD25 | AF21 | SysAD1 |
| AD20 | SysAD5 | AE12 | DDP1 | AF4 | DD22 | AF22 | SysADC2 |
| AD21 | SysAD3 | AE13 | SysAD29 | AF5 | DD18 | AF23 | SysCmd7 |
| AD22 | SysAD0 | AE14 | SysAD25 | AF6 | DD15 | AF24 | SysCmd3 |
| AD23 | SysADC0 | AE15 | SysAD21 | AF7 | DD11 | AF25 | GND |
| AD24 | GND | AE16 | SysAD18 | AF8 | DD8 | AF26 | GND |

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# 1. Pin Characteristics

## 1.1 Pin Functions

***Table 1-1: Pin Function (1/4)***

| Pin Name | I/O | Function | Interface |
|---|---|---|---|
| ClockIn | Input | Bonito clock buffer input (only connected to ClockOut (5:0)) | Clock buffer signals |
| ClockOut (5:0) | Output | Low skew clock outputs; each should have only one load; all should have the same track length on the board | |
| SysAD(31:0) | I/O | MIPS multiplexed bus | CPU interface signals |
| SysADC(3:0) | I/O | Parity check bits **Note 1** | |
| SysCmd(8:0) | I/O | Transfer type code | |
| $\overline{\text{EValid}}$/$\overline{\text{ValidIn}}$ | Output | Active, when Bonito drives the SysAD bus | |
| $\overline{\text{PValid}}$/$\overline{\text{ValidOut}}$ | Input | Active, when CPU drives the SysAD bus | |
| $\overline{\text{EOK}}$ | Output | CPU cycle flow control **Note 2** | |
| $\overline{\text{PMaster}}$/$\overline{\text{Release}}$ | Input | Active when the CPU stops driving the bus in a read cycle | |
| CPUClock | Input | Identical to the CPU's master clock | |
| $\overline{\text{SysReset}}$ | Input | Reset for Bonito and other circuits | |
| $\overline{\text{SysController}}$ | Input | Configuration signal; when low, Bonito drives the PCI bus $\overline{\text{Reset}}$ signal; when high, PCI bus $\overline{\text{Reset}}$ becomes an input and itself resets all functions in Bonito | |
| $\overline{\text{CPUColdReset}}$ | Output | Control signal for CPU's $\overline{\text{ColdReset}}$ input | |
| $\overline{\text{CPUReset}}$ | Output | Control signal for CPU's $\overline{\text{Reset}}$ input | |
| VCCOk | Output | Control signal for CPU's VCCOk input | |
| ModeClock | Input | Clock input from CPUs that use serial EPROM for configuration data | |
| ModeIn | Output | Data output to CPUs that use serial EPROM for configuration data | |

**Notes: 1.** Some MIPS based CPUs do not use parity on the SysAD bus; in these cases SysADC(3:0) can be left open.

**2.** For MIPS based CPUs with separate $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ pins $\overline{\text{RdRdy}}$ should be held permanently active and $\overline{\text{EOK}}$ should be connected to $\overline{\text{WrRdy}}$.

**3.** If an external PCI arbiter is used $\overline{\text{GNT0}}$ serves as Bonito's PCI request signal and $\overline{\text{REQ0}}$ serves as grant signal.

**4.** For large memory systems that require an external high-drive register, all shared signals (MUX(13:0), DBA(1:0), $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, $\overline{\text{DCKE}}$, $\overline{\text{DCS(1:0)H}}$ and $\overline{\text{DCS(1:0)L}}$) should be passed through the register.

**5.** During accesses on the local I/O bus these signals serve partly as address bus.

**6.** Normally connected to a zero-delay switch.

**7.** These pins are inputs while $\overline{\text{SysReset}}$ is active and can be used to make pre-reset chip configuration settings.

**8.** $\overline{\text{ROMCS1}}$ is the "default" bootstrap region.

*Table 1-1: Pin Function (2/4)*

| Pin Name | I/O | Function | Interface |
|---|---|---|---|
| $\overline{\text{Int(1:0)}}$ | Output | Interrupt outputs to CPU | CPU interface signals |
| CLK | Input | PCI bus clock | PCI bus signals |
| AD(31:0) | I/O | PCI address and data | |
| PAR | I/O | Parity | |
| $\overline{\text{CBE(3:0)}}$ | I/O | PCI cycle type (during address cycle) or byte-enables (during data cycle) | |
| $\overline{\text{DEVSEL}}$ | I/O | PCI device select signal; asserted when a PCI target is accessed | |
| $\overline{\text{FRAME}}$ | I/O | Asserted when PCI initiator starts a transaction | |
| $\overline{\text{IRDY}}$ | I/O | PCI initiator ready signal; asserted when the PCI initiator is in data enable state | |
| $\overline{\text{STOP}}$ | I/O | PCI stop signal; asserted when target signals the initiator to stop the transaction | |
| $\overline{\text{TRDY}}$ | I/O | PCI target ready signal; asserted when the target is in transfer enable state | |
| $\overline{\text{LOCK}}$ | Input | PCI exclusive access control | |
| $\overline{\text{PERR}}$ | I/O | PCI parity error reporting signal | |
| $\overline{\text{SERR}}$ | I/O | PCI general error reporting signal | |
| $\overline{\text{RESET}}$ | I/O | PCI reset signal (see description of $\overline{\text{SysController}}$ signal) | |
| IDSEL | Input | Indicates incoming PCI configuration cycles | |
| $\overline{\text{IRQA}}$ | I/O | Can be configured as input to Bonito's interrupt controller or as open collector output | |
| $\overline{\text{REQ(5:0)}}$ | Input | PCI bus request signal **Note 3** | |
| $\overline{\text{GNT(5:0)}}$ | Output | PCI bus grant signal **Note 3** | |
| MUX(13:0) | Output | Multiplexed addresses **Note 4** | SDRAM interface signals |
| DBA(1:0) | Output | Bank select signals | |
| DB(31:0) | I/O | SDRAM data bus **Note 5** | |
| DDP(3:0) | I/O | Parity/check bits for data bus | |
| $\overline{\text{DRAS}}$ | Output | RAS signal for SDRAM | |

**Notes: 1.** Some MIPS based CPUs do not use parity on the SysAD bus; in these cases SysADC(3:0) can be left open.

**2.** For MIPS based CPUs with separate $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ pins $\overline{\text{RdRdy}}$ should be held permanently active and $\overline{\text{EOK}}$ should be connected to $\overline{\text{WrRdy}}$.

**3.** If an external PCI arbiter is used $\overline{\text{GNT0}}$ serves as Bonito's PCI request signal and $\overline{\text{REQ0}}$ serves as grant signal.

**4.** For large memory systems that require an external high-drive register, all shared signals (MUX(13:0), DBA(1:0), $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, $\overline{\text{DCKE}}$, $\overline{\text{DCS(1:0)H}}$ and $\overline{\text{DCS(1:0)L}}$) should be passed through the register.

**5.** During accesses on the local I/O bus these signals serve partly as address bus.

**6.** Normally connected to a zero-delay switch.

**7.** These pins are inputs while $\overline{\text{SysReset}}$ is active and can be used to make pre-reset chip configuration settings.

**8.** $\overline{\text{ROMCS1}}$ is the "default" bootstrap region.

*Table 1-1: Pin Function (3/4)*

| Pin Name | I/O | Function | Interface |
|---|---|---|---|
| $\overline{\text{DCAS}}$ | Output | CAS signal for SDRAM | SDRAM interface signals |
| $\overline{\text{DWE}}$ | Output | WE signal for SDRAM | |
| $\overline{\text{DCKE}}$ | Output | CKE signal for SDRAM | |
| $\overline{\text{DCS(1:0)H}}$ | Output | CS signals two physical banks of SDRAM | |
| $\overline{\text{DCS(1:0)L}}$ | Output | CS signals two physical banks of SDRAM | |
| DQMBLo | Output | Byte enable signal for lower 32-bit half of SDRAM | |
| DQMBHi | Output | Byte enable signal for upper 32-bit half of SDRAM | |
| $\overline{\text{DDMuxHi}}$ | Output | Control signal to multiplex upper half of 64-bit DIMM modules to Bonito's 32-bit SDRAM data bus **Note 6** | |
| $\overline{\text{DDMuxLo}}$ | Output | Control signal to multiplex lower half of 64-bit DIMM modules to Bonito's 32-bit SDRAM data bus **Note 6** | |
| IOD(15:0) | I/O | Local bus data lines **Note 7** | I/O and ROM interface signals |
| IOA(4:0) | Output | Local bus low order address bits | |
| Isolate | Output | Control signal to isolate ROM signals from high-speed SDRAM signals | |
| $\overline{\text{ROMCS(1:0)}}$ | I/O | Chip select signals for ROM devices **Note 8** | |
| $\overline{\text{IOCS(3:0)}}$ | Output | Chip select signals for I/O devices | |
| $\overline{\text{IORD}}$ | Output | Read strobe signal for ROM and I/O devices | |
| $\overline{\text{IOWR}}$ | Output | Write strobe signal for ROM and I/O devices | |
| IORDY | Input | I/O channel ready signal | |
| DMARQ | Input | DMA request signal | I/O bus DMA and IDE support |
| $\overline{\text{DMACK}}$ | Output | DMA acknowledge signal | |
| IODIR | Output | Direction control signal (high for write) | |
| $\overline{\text{IODEN}}$ | Output | Enable control signal for external data buffer | |
| GPIO(8:0) | I/O | General purpose programmable I/O ports | Programmable I/O signals |
| GPIn(5:0) | Input | Interrupt or general purpose input pins | |

**Notes: 1.** Some MIPS based CPUs do not use parity on the SysAD bus; in these cases SysADC(3:0) can be left open.

**2.** For MIPS based CPUs with separate $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ pins $\overline{\text{RdRdy}}$ should be held permanently active and $\overline{\text{EOK}}$ should be connected to $\overline{\text{WrRdy}}$.

**3.** If an external PCI arbiter is used $\overline{\text{GNT0}}$ serves as Bonito's PCI request signal and $\overline{\text{REQ0}}$ serves as grant signal.

**4.** For large memory systems that require an external high-drive register, all shared signals (MUX(13:0), DBA(1:0), $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, $\overline{\text{DCKE}}$, $\overline{\text{DCS(1:0)H}}$ and $\overline{\text{DCS(1:0)L}}$) should be passed through the register.

**5.** During accesses on the local I/O bus these signals serve partly as address bus.

**6.** Normally connected to a zero-delay switch.

**7.** These pins are inputs while $\overline{\text{SysReset}}$ is active and can be used to make pre-reset chip configuration settings.

**8.** $\overline{\text{ROMCS1}}$ is the "default" bootstrap region.

*Table 1-1: Pin Function (4/4)*

| Pin Name | I/O | Function | Interface |
|---|---|---|---|
| JTCK | Input | JTAG clock input | Programmable I/O signals |
| JTDI | Input | JTAG data input | |
| JTDO | Output | JTAG data output | |
| JTMS | Input | JTAG mode select signal | |
| GND | Input | Ground | Power and generic signals |
| $V_{DD}$ | Input | Supply voltage | |
| $V_{D5}$ | Input | Supply voltage for PCI bus I/Os | |
| TEST(2:0) | Input | Reserved, leave open | Test pins |
| TMD(2:0) | Input | Reserved, connect to GND via pull-down | |
| SMC | Input | Reserved, leave open | |

**Notes: 1.** Some MIPS based CPUs do not use parity on the SysAD bus; in these cases SysADC(3:0) can be left open.

**2.** For MIPS based CPUs with separate $\overline{\text{RdRdy}}$ and $\overline{\text{WrRdy}}$ pins $\overline{\text{RdRdy}}$ should be held permanently active and $\overline{\text{EOK}}$ should be connected to $\overline{\text{WrRdy}}$.

**3.** If an external PCI arbiter is used $\overline{\text{GNT0}}$ serves as Bonito's PCI request signal and $\overline{\text{REQ0}}$ serves as grant signal.

**4.** For large memory systems that require an external high-drive register, all shared signals (MUX(13:0), DBA(1:0), $\overline{\text{DRAS}}$, $\overline{\text{DCAS}}$, $\overline{\text{DWE}}$, $\overline{\text{DCKE}}$, $\overline{\text{DCS(1:0)H}}$ and $\overline{\text{DCS(1:0)L}}$) should be passed through the register.

**5.** During accesses on the local I/O bus these signals serve partly as address bus.

**6.** Normally connected to a zero-delay switch.

**7.** These pins are inputs while $\overline{\text{SysReset}}$ is active and can be used to make pre-reset chip configuration settings.

**8.** $\overline{\text{ROMCS1}}$ is the "default" bootstrap region.

## 1.2 Pin Status and Recommended Connection Examples

*Table 1-2: Pin Status and Recommended Connection Examples (1/3)*

| Pin Name | I/O | Drive Capacity (mA) | Withstand Voltage (V) | Internal Processing | External Processing | Status during Reset |
|---|---|---|---|---|---|---|
| **Clock buffer signals** | | | | | | |
| Clockin | I | | 3.3 V | | | - |
| ClockOut(5:0) | O | 9 | 3.3 V | | | |
| **CPU interface signals** | | | | | | |
| SysAD(31:0) | I/O | 6 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| SysADC(3:0) | I/O | 6 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| SysCmd(8:0) | I/O | 6 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| $\overline{\text{EValid}}$/$\overline{\text{ValidIn}}$ | O | 6 | 3.3 V | | | H |
| $\overline{\text{PValid}}$/$\overline{\text{ValidOut}}$ | I | | 3.3 V | | | – |
| $\overline{\text{EOK}}$ | O | 6 | 3.3 V | | | H |
| $\overline{\text{Pmaster}}$/$\overline{\text{Release}}$ | I | | 3.3 V | 50 KΩ Pull-up | | – |
| $\overline{\text{SysReset}}$ | I | | 5 V TOL | | | – |
| $\overline{\text{SysController}}$ | I | | 3.3 V | | | – |
| $\overline{\text{CPU Reset}}$ | O | 6 | 3.3 V | 50 KΩ Pull-down | | L |
| VCCOk | O | 6 | 3.3 V | 50 KΩ Pull-down | | L |
| ModeClock | I | | 3.3 V | 50 KΩ Pull-down | | – |
| ModeIn | O | 6 | 3.3 V | 50 KΩ Pull-down | | L |
| $\overline{\text{Int(1:0)}}$ | O | 6 | 3.3 V | 50 KΩ Pull-up | | H |
| **PCI interface signals** | | | | | | |
| CLK | I | | 5 V TOL | | | – |
| AD(31:0) | I/O | PCI | 5 V TOL | | | Hi-Z |
| PAR | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{CBE(3:0)}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{DEVSEL}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{FRAME}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{IRDY}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{STOP}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{TRDY}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{LOCK}}$ | I | | 5 V TOL | | | – |
| $\overline{\text{PERR}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{SERR}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{RESET}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| IDSEL | I | | 5 V TOL | | | – |
| $\overline{\text{IRQA}}$ | I/O | PCI | 5 V TOL | | | Hi-Z |
| $\overline{\text{REQ(5:0)}}$ | I | | 5 V TOL | | | – |
| $\overline{\text{GNT(5:0)}}$ | O | PCI | 5 V TOL | | | H |

*Table 1-2: Pin Status and Recommended Connection Examples (2/3)*

| Pin Name | I/O | Drive Capacity (mA) | Withstand Voltage (V) | Internal Processing | External Processing | Status during Reset |
|---|---|---|---|---|---|---|
| **SDRAM interface signals** | | | | | | |
| MUX(13:0) | O | 12 | 3.3 V | | | undefined |
| DBA(1:0) | O | 12 | 3.3 V | | | undefined |
| DD(31:0) | I/O | 12 | 3.3 V | | | Hi-Z |
| DDP(3:0) | I/O | 12 | 3.3 V | | | Hi-Z |
| $\overline{\text{DRAS}}$ | O | 12 | 3.3 V | | | H |
| $\overline{\text{DCAS}}$ | O | 12 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| $\overline{\text{DWE}}$ | O | 12 | 3.3 V | | | H |
| DCKE | O | 12 | 3.3 V | | | H |
| $\overline{\text{DCS(1:0)H}}$ | O | 12 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| $\overline{\text{DCS(1:0)L}}$ | O | 12 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| DQMBLo | O | 12 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| DQMBHi | O | 12 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| $\overline{\text{DDMuxHi}}$ | O | 12 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| $\overline{\text{DDMuxLo}}$ | O | 12 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| **I/O and ROM interface signals** | | | | | | |
| IOD(15:0) | I/O | 9 | 5 V TOL | 50 KΩ Pull-down | | Hi-Z |
| IOA(4:0) | O | 9 | 3.3 V | | | undefined |
| Isolate | O | 6 | 3.3 V | 50 KΩ Pull-down | | Hi-Z |
| $\overline{\text{RomCS(1:0)}}$ | I/O | 9 | 5 V TOL | 50 KΩ Pull-down | | Hi-Z |
| $\overline{\text{IOCS(3:0)}}$ | O | 6 | 3.3 V | 50 KΩ Pull-down | | Hi-Z |
| $\overline{\text{IORd}}$ | O | 9 | 3.3 V | 50 KΩ Pull-down | | Hi-Z |
| $\overline{\text{IOWr}}$ | O | 9 | 3.3 V | 50 KΩ Pull-down | | Hi-Z |
| IORDY | I | | 5 V TOL | Schmitt | | – |
| **I/O bus DMA and IDE support** | | | | | | |
| DMARQ | I | | 5 V TOL | 50 KΩ Pull-down | | – |
| $\overline{\text{DMACK}}$ | O | 9 | 3.3 V | 50 KΩ Pull-down | | Hi-Z |
| IODIR | O | 6 | 3.3 V | | | L |
| $\overline{\text{IODEN}}$ | O | 6 | 3.3 V | 50 KΩ Pull-up | | Hi-Z |
| **Programmable IO signals** | | | | | | |
| GPIO(8:0) | I/O | 9 | 5 V TOL | 50 KΩ Pull-down | | Hi-Z |
| GPIn(5:0) | I | | 5 V TOL | 50 KΩ Pull-down | | – |
| **JTAG signals** | | | | | | |
| JTCK | I | | 3.3 V | | | – |
| JTDI | I | | 3.3 V | 50 KΩ Pull-up | | – |
| JTDO | O | 6 | 3.3 V | | | |
| JTMS | I | | 3.3 V | 50 KΩ Pull-up | | – |

*Table 1-2: Pin Status and Recommended Connection Examples (3/3)*

| Pin Name | I/O | Drive Capacity (mA) | Withstand Voltage (V) | Internal Processing | External Processing | Status during Reset |
|---|---|---|---|---|---|---|
| **Test pins** | | | | | | |
| TEST(2:0) | I | | | pull-down | leave open | |
| TMD(2:0) | I | | | - | connect to GND via external pull-down | |
| SMC | I | | | pull-up | leave open | |

# 2. Electrical Specifications

## 2.1 Absolute Maximum Ratings

**($T_A$ = +25°C)**

***Table 2-1: Absolute Maximum Ratings***

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | | -0.5 to +4.6 | V |
| Input voltage | $V_I$ | | | |
| LVTTL input buffer | | $V_I < V_{DD}$ + 0.5 V | -0.5 to +4.6 | V |
| LVTTL input buffer with fail-safe function | | $V_I < V_{DD}$ + 0.5 V | -0.5 to +4.6 | V |
| TTL 5 V withstand voltage input buffer | | $V_I < V_{DD}$ + 3.0 V | -0.5 to +6.6 | V |
| Output voltage | $V_O$ | | | |
| LVTTL output buffer | | $V_O < V_{DD}$ + 0.5 V | -0.5 to +4.6 | V |
| TTL 5 V withstand voltage output buffer | | $V_O < V_{DD}$ + 3.0 V | -0.5 to +6.6 | V |
| CMOS 5 V withstand voltage output buffer | | $V_O < V_{DD}$ + 3.0 V | -0.5 to +6.6 | V |
| Output current | $I_O$ | | | |
| $I_{OL}$ = 1.0 mA | | | 3 | mA |
| $I_{OL}$ = 2.0 mA | | | 7 | mA |
| $I_{OL}$ = 3.0 mA | | | 10 | mA |
| $I_{OL}$ = 6.0 mA | | | 20 | mA |
| $I_{OL}$ = 9.0 mA | | | 30 | mA |
| $I_{OL}$ = 12.0 mA | | | 40 | mA |
| $I_{OL}$ = 18.0 mA | | | 60 | mA |
| $I_{OL}$ = 24.0 mA | | | 75 | mA |
| Storage temperature | $T_{stg}$ | | -65 to +150 | °C |
| Operating ambient temperature | $T_A$ | | -40 to +85 | °C |

**Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.**

**Remark:** Except for buffers with the fail-safe function, 5 V or 3.3 V must be applied to the I/O pins only after applying the power supply voltage.

## 2.2 General Characteristics

*Table 2-2: Capacitance of Interface Block ($C_B$)*

| Parameter | Symbol | Conditions | MIN. | MAX. | Unit |
|---|---|---|---|---|---|
| Input buffer | $C_B$ | $V_{DD}$ = 0 V; $T_J$ = 25°C; f = 1 MHz<br>Unmeasured pins returned to 0 V | | | |
| LVTTL (Normal) | | | 3.25 | 3.97 | pF |
| LVTTL (With Fail-Safe) | | | 2.84 | 3.48 | pF |
| 5 V withstand voltage | | | 6.25 | 6.97 | pF |

| Interface Level | | $C_B$ (pF) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 1 mA | 2 mA | 3 mA | 6 mA | 9 mA | 12 mA | 18 mA | 24 mA |
| Output buffer/<br>bi-directional buffer | | | | | | | | | |
| LVTTL | MIN. | -- | -- | 3.25 | 3.25 | 3.25 | 3.25 | 3.25 | 3.25 |
| | MAX. | -- | -- | 3.97 | 3.97 | 3.97 | 3.97 | 3.97 | 3.97 |
| 5 V withstand voltage | MIN. | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 |
| | MAX. | 6.97 | 6.97 | 6.97 | 6.97 | 6.97 | 6.97 | 6.97 | 6.97 |
| CMOS 5 V withstand voltage | MIN. | -- | -- | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 |
| | MAX. | -- | -- | 6.97 | 6.97 | 6.97 | 6.97 | 6.97 | 6.97 |

**Remarks: 1.** $V_{DD}$ = 0 V; $T_J$ = 25°C; f = 1 MHz

**2.** Add the capacitance of the input buffer for the bi-directional buffer.

*Table 2-3: Capacitance of Package ($C_P$)*

| Package | | Lead Pitch | Chip Size | $C_P$ (pF) |
|---|---|---|---|---|
| Plastic BGA | 100 | 1.27 mm, perimeter | 35 x 35 mm | 1.3 to 1.5 |

## 2.3 Operating Conditions

***Table 2-4: Recommended Operating Conditions***

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3 | 3.3 | 3.6 | V |
| 5 V Supply voltage | $V_{D5}$ | 4.5 | 5 | 5.5 | V |
| Ambient temperature | $T_A$ | -40 | | +85 | °C |

***Table 2-5: Recommended Operating Range***

| Parameter | Symbol | Conditions | | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | | | 3.0 | 3.3 | 3.6 | V |
| High-level input voltage | $V_{IH}$ | LVTTL input buffer | | 2.0 | | $V_{DD}$ | V |
| Low-level input voltage | $V_{IL}$ | LVTTL input buffer with fail-safe function | | 0 | | 0.8 | V |
| Positive trigger voltage | $V_P$ | | Schmitt input | 1.4 | | 2.4 | V |
| Negative trigger voltage | $V_N$ | | | 0.8 | | 1.6 | V |
| Hysteresis voltage | $V_H$ | | | 0.3 | | 1.5 | V |
| High-level input voltage | $V_{IH}$ | TTL 5 V withstand voltage input buffer | | 2.0 | | 5.5 | V |
| Low-level input voltage | $V_{IL}$ | | | 0 | | 0.8 | V |
| Positive trigger voltage | $V_P$ | | Schmitt input | 1.4 | | 2.4 | V |
| Negative trigger voltage | $V_N$ | | | 0.8 | | 1.6 | V |
| Hysteresis voltage | $V_H$ | | | 0.3 | | 1.5 | V |
| Input rise time | $t_{ri}$ | Normal input | | 0 | | 200 | ns |
| Input fall time | $t_{fi}$ | | | 0 | | 200 | ns |
| Input rise time | $t_{ri}$ | Schmitt input | | 0 | | 10 | ms |
| Input fall time | $t_{fi}$ | | | 0 | | 10 | ms |

## 2.4 DC Characteristics

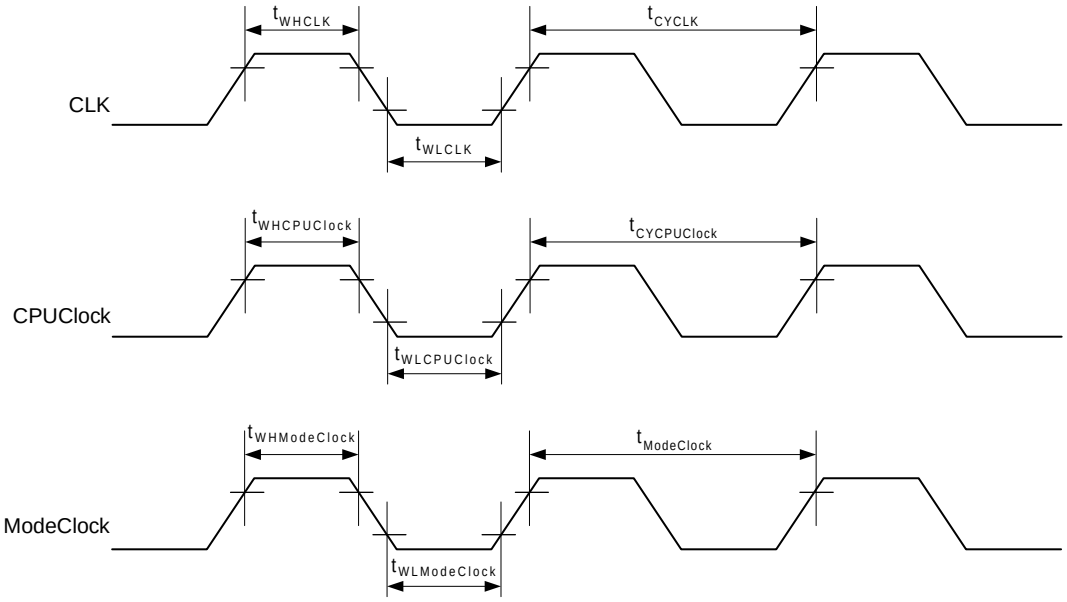
### 2.4.1 Clock Parameters

*Table 2-6: Clock Parameters*

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| CLK clock cycle time | $t_{CYCLK}$ | | 30 | | 125 | ns |
| CLK clock high-level width | $t_{WHCLK}$ | | 11 | | | ns |
| CLK clock low-level width | $t_{WLCLK}$ | | 11 | | | ns |
| CLK slew rate | | between 0.2 $V_{DD}$ and 0.6 $V_{DD}$ | 1 | | 4 | ns |
| ClockIn clock cycle time | $t_{CYClockIn}$ | | 11 | | | ns |
| ClockOut0-5 delay | $t_{DClockOut}$ | | 1.6 | | 4.2 | ns |
| ClockOut0-5 skew | | | | | 140 | ps |
| CPUClock clock cycle time | $t_{CYCPUClock}$ | | 11 | | 30 | ns |
| CPUClock high-level width | $t_{WHCPUClock}$ | | 4.3 | | - | ns |
| CPUClock low-level width | $t_{WLCPUClock}$ | | 3.3 | - | - | ns |
| ModeClock clock cycle time | $t_{CYModeclock}$ | fixed to 256 × CPU Clock cycle time**Note** | | | | |
| ModeClock high-level width | $t_{WHModeClock}$ | | 3 | - | - | CPU clock cycles |
| ModeClock low-level width | $t_{WLModeClock}$ | | 3 | - | - | CPU clock cycles |

**Note:** $t_{CYModeclock} = 256 \times t_{CYCPUClock}$

***Figure 2-1: Clock Waveforms***



### 2.4.2 PCI Interface Parameters

*Table 2-7: PCI Interface Parameters*

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| AD(31:0) valid delay time (from CLK) | $t_{DAD}$ | | 2 | | 11.1 | ns |
| AD(31:0) setup time (to CLK) | $t_{SAD}$ | | 7 | | | ns |
| AD(31:0) hold time (from CLK) | $t_{HAD}$ | | 0.04 | | | ns |
| $\overline{CBE(3:0)}$, $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{STOP}$, PAR, $\overline{DEVSEL}$, $\overline{SERR}$, $\overline{PERR}$ valid delay time | $t_{DCBE}$ | | 2 | | 11.1 | ns |
| $\overline{CBE(3:0)}$, $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{STOP}$, PAR, $\overline{DEVSEL}$, IDSEL setup time (to CLK) | $t_{SCBE}$ | | 7 | | | ns |
| $\overline{CBE(3:0)}$, $\overline{FRAME}$, $\overline{TRDY}$, $\overline{IRDY}$, $\overline{STOP}$, PAR, $\overline{DEVSEL}$, IDSEL hold time (from CLK) | $t_{HCBE}$ | | 0.04 | | | ns |
| Reset Active Time after Power stable | - | | 4 | | | CLK clocks |
| Reset Active Time after CLK stable | - | | 4 | | | CLK clocks |
| $\overline{GNT(5:0)}$ valid delay time (from CLK) **Note** | $t_{DGNT}$ | | 3.0 | | 9.0 | ns |
| $\overline{REQ(5:0)}$ setup time (to CLK) **Note** | $t_{SREQ}$ | | 10 | | | ns |
| $\overline{REQ(5:0)}$ hold time (from CLK)**Note** | $t_{HREQ}$ | | 0 | | | ns |

**Note:** The REQ/GNT timings are given for Bonito's arbiter being used. In case that Bonito's arbiter is not used, the $\overline{GNT0}$ pin provides the REQ signal and the $\overline{REQ0}$ pin provides the GNT signal, so that the same signal timings apply.

*Figure 2-2: PCI Output Timing*

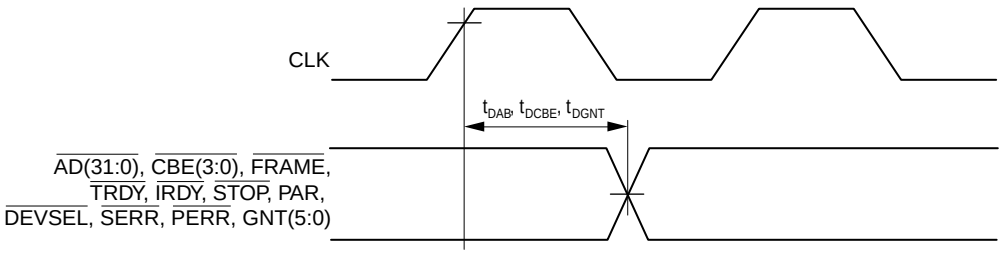
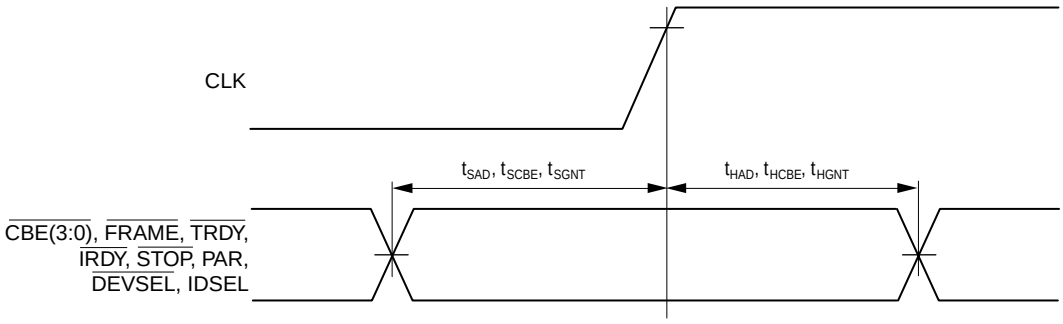


*Figure 2-3: PCI Input Timing*

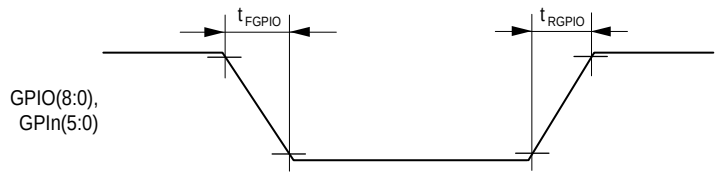



### 2.4.3 GPIO and Interrupt Parameters

*Table 2-8: GPIO and Interrupt Parameters*

| Parameter | Symbol | Conditions | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|---|
| input level width to detect an interrupt | | | 3 | | | CPU clock cycles |
| Switching time from level interrupt input to output | | | | | 3 | |
| Switching time from edge interrupt input to output | | | | | 5 | |
| GPIO(8:0) and GPIn (5:0) rise time | $t_{RGPIO}$ | | 0 | | 200 | ns |
| GPIO(8:0) and GPIn (5:0) fall time | $t_{FGPIO}$ | | 0 | | 200 | ns |
| Output level width | software controlled | | | | | |

*Figure 2-4: GPIO and Interrupt Parameters*



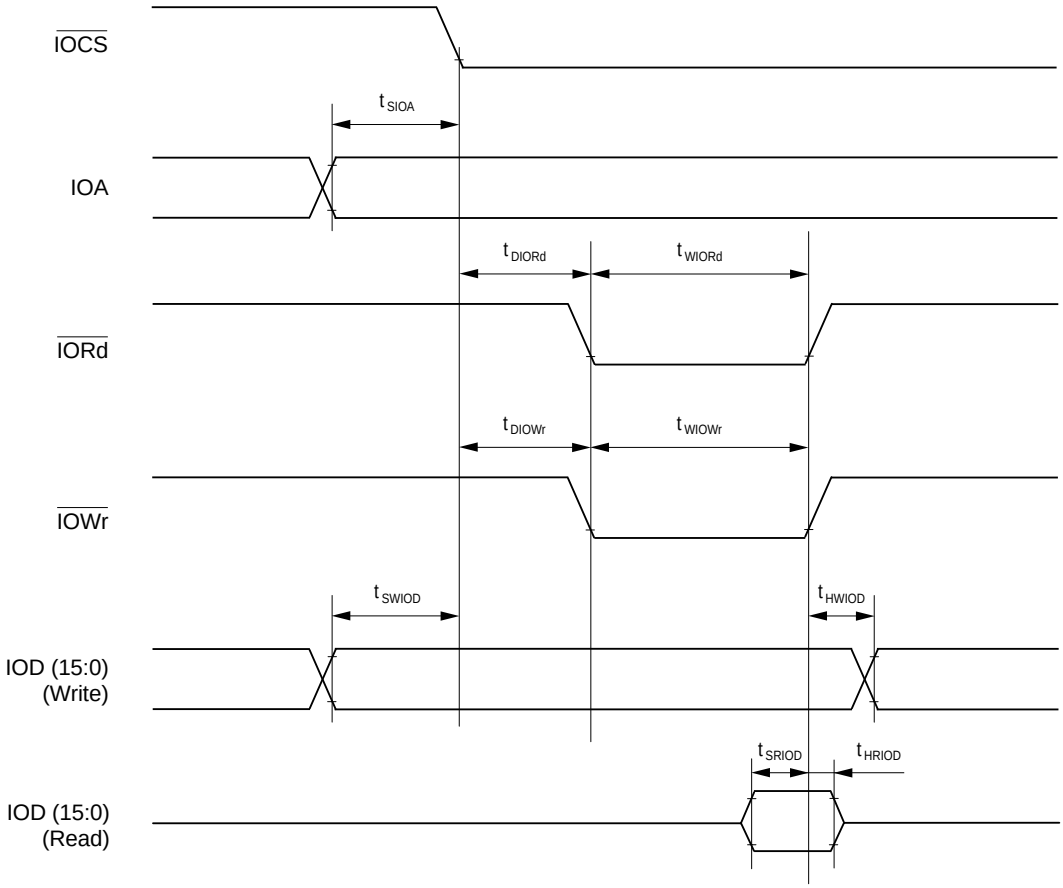
### 2.4.4 Local I/O Bus Interface

***Table 2-9: Local I/O Bus Timing Parameters***

| Parameter | | Symbol | Conditions | TYP. | Units |
|---|---|---|---|---|---|
| Address setup time (IOA valid to $\overline{IOCS}$ low) | | $t_{SIOA}$ | | 2 | $T_{iocyc}$ |
| Address hold time | | $t_{HIOA}$ | | 1 | $T_{iocyc}$ |
| Read data setup time | | $t_{SRIOD}$ | | 2 | $T_{iocyc}$ |
| Read data hold time | | $t_{HRIOD}$ | | 0 | $T_{iocyc}$ |
| Write data setup time (IOD valid to $\overline{IOCS}$ low) | | $t_{SWIOD}$ | | 2 | $T_{iocyc}$ |
| Write data hold time | | $t_{HWIOD}$ | | 1 | $T_{iocyc}$ |
| $\overline{IORd}$ delay time ($\overline{IOCS}$ low to $\overline{IORd}$ low) | | $t_{DIORd}$ | | 2 | $T_{iocyc}$ |
| $\overline{IOWr}$ delay time ($\overline{IOCS}$ low to $\overline{IOWr}$ low) | | $t_{DIOWr}$ | | 2 | $T_{iocyc}$ |
| $\overline{IORd}$ pulse width (low) | ROM cycles | $t_{WIORd}$ | | 4/7 | $T_{iocyc}$ |
| | I/O cycles | $t_{WIORd}$ | | 11/26 | $T_{iocyc}$ |
| $\overline{IOWr}$ pulse width (low) | ROM cycles | $t_{WIOWr}$ | | 4/7 | $T_{iocyc}$ |
| | I/O cycles | $t_{WIOWr}$ | | 11/26 | $T_{iocyc}$ |

**Remark:** All timings are given in terms of Tiocyc which is 2 times the CPU clock period.
The $\overline{IORd}$/$\overline{Wr}$ widths are written as <fast cycle>/<slow cycle> which can be programmed in Bonito's iodevCfg register.

***Figure 2-5: Local I/O Bus Timing Parameters***



### 2.4.5 SDRAM Interface

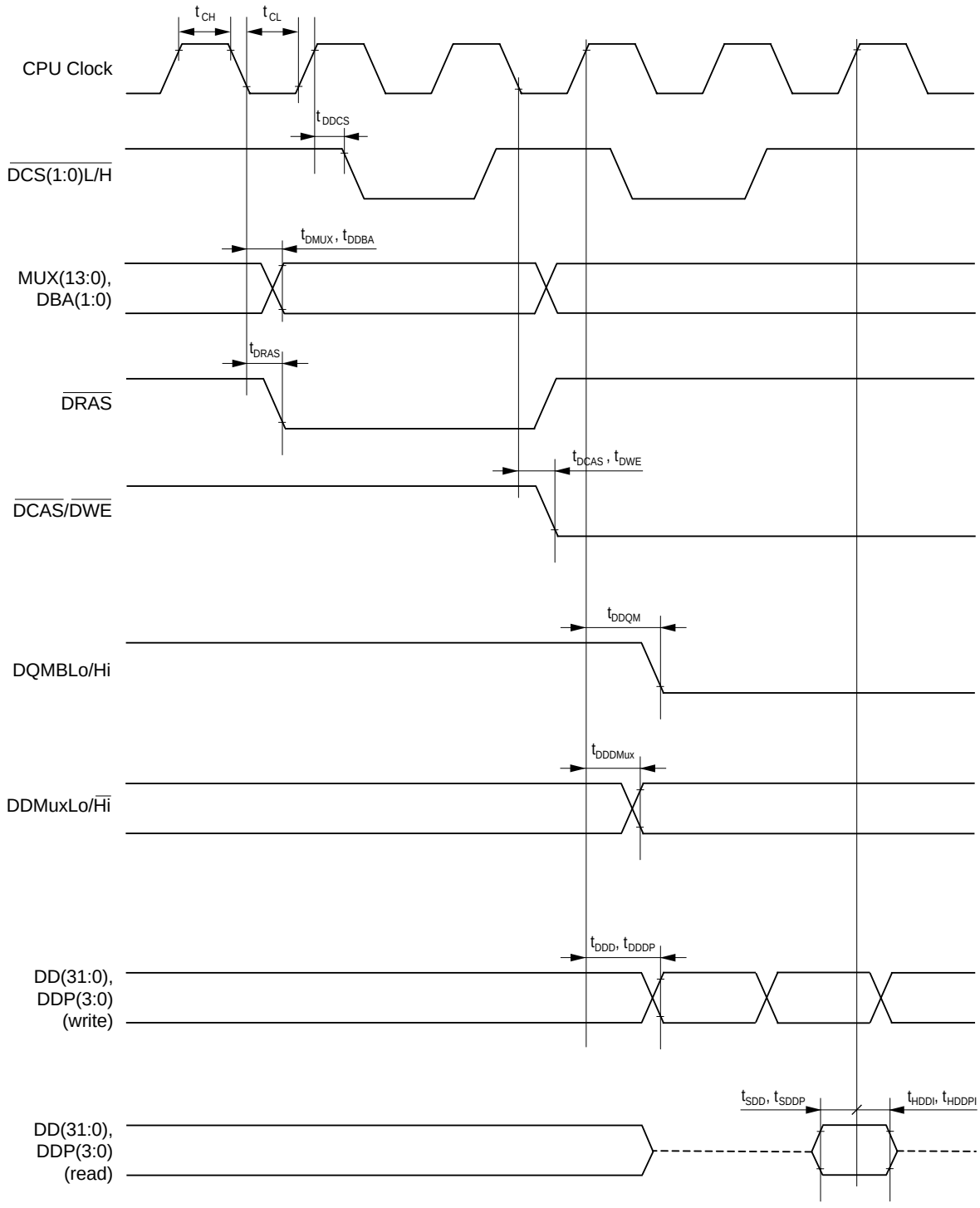
*Table 2-10: SDRAM Interface Timing Parameters*

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| MUX(13:0) clock-to-output delay time | $t_{DMUX}$ | 2.0 | | 6.0 | ns |
| DBA(1:0) clock-to-output delay time | $t_{DDBA}$ | 2.0 | | 6.0 | ns |
| DD(31:0) clock-to-output delay time | $t_{DDD}$ | 3.0 | | 9.6 | ns |
| DD(31:0) output hold time | $t_{HDDO}$ | 3.0 | | | ns |
| DDP(3:0) clock-to-output delay time | $t_{DDDP}$ | 3.2 | | 10.0 | ns |
| DDP(3:0) output hold time | $t_{HDDPO}$ | 3.2 | | | ns |
| DD(31:0) input setup time | $t_{SDD}$ | 2.1 | | | ns |
| DD(31:0) input hold time | $t_{HDDI}$ | 0 | | | ns |
| DDP(3:0) input setup time | $t_{SDDP}$ | 2.1 | | | ns |
| DDP(3:0) input hold time | $t_{HDDPI}$ | 0 | | | ns |
| $\overline{\text{DRAS}}$ clock-to-output delay time | $t_{DRAS}$ | 3.5 | | 7.5 | ns |
| $\overline{\text{DCAS}}$ clock-to-output delay time | $t_{DCAS}$ | 2.5 | | 6.0 | ns |
| $\overline{\text{DWE}}$ clock-to-output delay time | $t_{DDWE}$ | 2.5 | | 6.2 | ns |
| $\overline{\text{DCS(1:0)L/H}}$ clock-to-output delay time | $t_{DDCS}$ | 2.0 | | 6.0 | ns |
| DQMBLo/Hi clock-to-output delay time | $t_{DDQM}$ | 2.1 | | 7.7 | ns |
| $\overline{\text{DDMuxLo/Hi}}$ clock-to-output delay time | $t_{DDDMux}$ | 1.5 | | 4.8 | ns |
| RD/WR to RD/WR command | | 1 | | | clocks |
| Mode register set to ACT command | | 3 | | | clocks |
| WR to output data | | 0 | | | clocks |
| DQM to WR data mask | | 0 | | | clocks |
| Last read/write data cycle to PRE command | | 1 | | | clocks |
| ACT to REF/ACT command period (Operation) | | 7 | | | clocks |
| REF to REF/ACT command period (Refresh) | | 9 | | | clocks |
| ACT to PRE command period | | 5 | | | clocks |
| PRE to ACT command period | | 2 | | | clocks |
| ACT to READ/WRITE command | | 2 | | | clocks |
| ACT (one) to ACT (another) command period | | 7 | | | clocks |
| Refresh time | | 6.825 μs @ 91 MHz | | | |

**Remark:** Bonito meets the PC100-222 SDRAM specification at its sign-off speed of 91 MHz. [222 means CAS latency = 2, ACT to CMD = 2, PRE to ACT = 2]. All PC133 SDRAMs meet PC100-222 when run @100 MHz and they have a much better loading specification on the control signals - RAS, CAS, MUXADDR etc.

Bonito only supports a CAS latency of 2.

***Figure 2-6: SDRAM Timing Parameters***



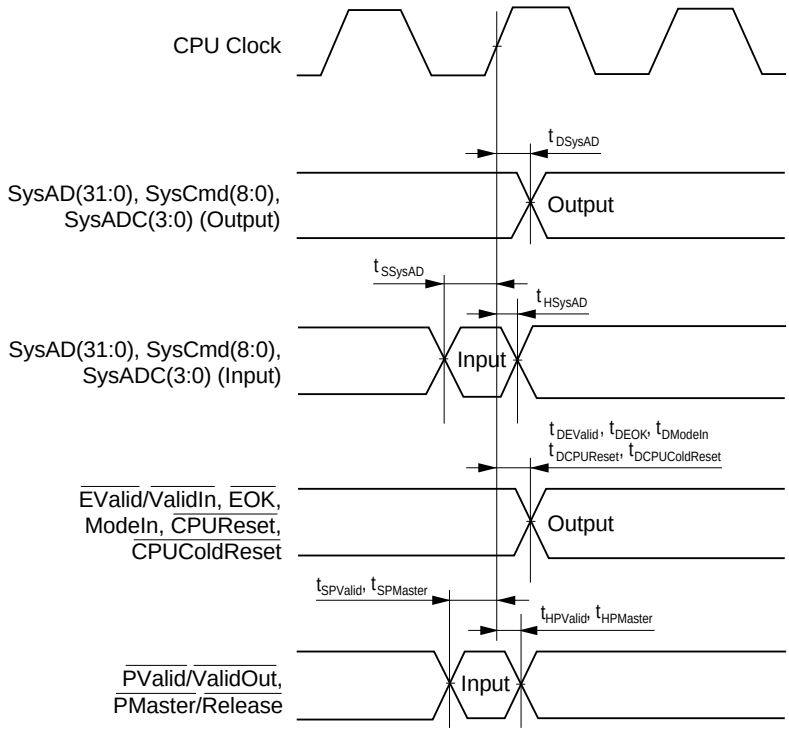
### 2.4.6 SYSAD Bus Interface

*Table 2-11: SysAD Bus Timing Parameters*

| Parameter | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| SysAD(31:0), SysADC(3:0), SysCmd (8:0) output delay time | $t_{DSysAD}$ | 1.7 | | 5.6 | ns |
| SysAD(31:0), SysADC(3:0), SysCmd (8:0) input setup time | $t_{SSysAD}$ | 3.4 | | | ns |
| SysAD(31:0), SysADC(3:0), SysCmd (8:0) input hold time | $t_{HSysAD}$ | 0 | | | ns |
| $\overline{\text{EValid}}$/$\overline{\text{Validin}}$ output delay time | $t_{DEValid}$ | 1.8 | | 6.0 | ns |
| $\overline{\text{PValid}}$/$\overline{\text{ValidOut}}$ input setup time | $t_{SPValid}$ | 3.4 | | | ns |
| $\overline{\text{PValid}}$/$\overline{\text{ValidOut}}$ input hold time | $t_{HPValid}$ | 0 | | | ns |
| $\overline{\text{EOK}}$ output delay time | $t_{DEOK}$ | 1.7 | | 5.6 | ns |
| $\overline{\text{PMaster}}$/$\overline{\text{Release}}$ input setup time | $t_{SPMaster}$ | 3.4 | | | ns |
| $\overline{\text{PMaster}}$/$\overline{\text{Release}}$ input hold time | $t_{HPMaster}$ | 0 | | | ns |
| $\overline{\text{SysReset}}$ input hold time | $t_{HSysReset}$ | 3 | | | CPU clocks |
| ModeIn output delay time | $t_{DModeIn}$ | 4.0 | | 15 | ns |
| $\overline{\text{CPUReset}}$ output delay time | $t_{DCPUReset}$ | 1.7 | | 4.9 | ns |
| CPUColdReset output delay time | $t_{DCPUColdReset}$ | 1.9 | | 5.2 | ns |

**Remark:** VCCOk and $\overline{\text{Int}}$(1:0) are async outputs; $\overline{\text{SYSReset}}$ and $\overline{\text{SYSController}}$ are async inputs. $\overline{\text{SysController}}$ has to be setup before $\overline{\text{SysReset}}$ disasserts.

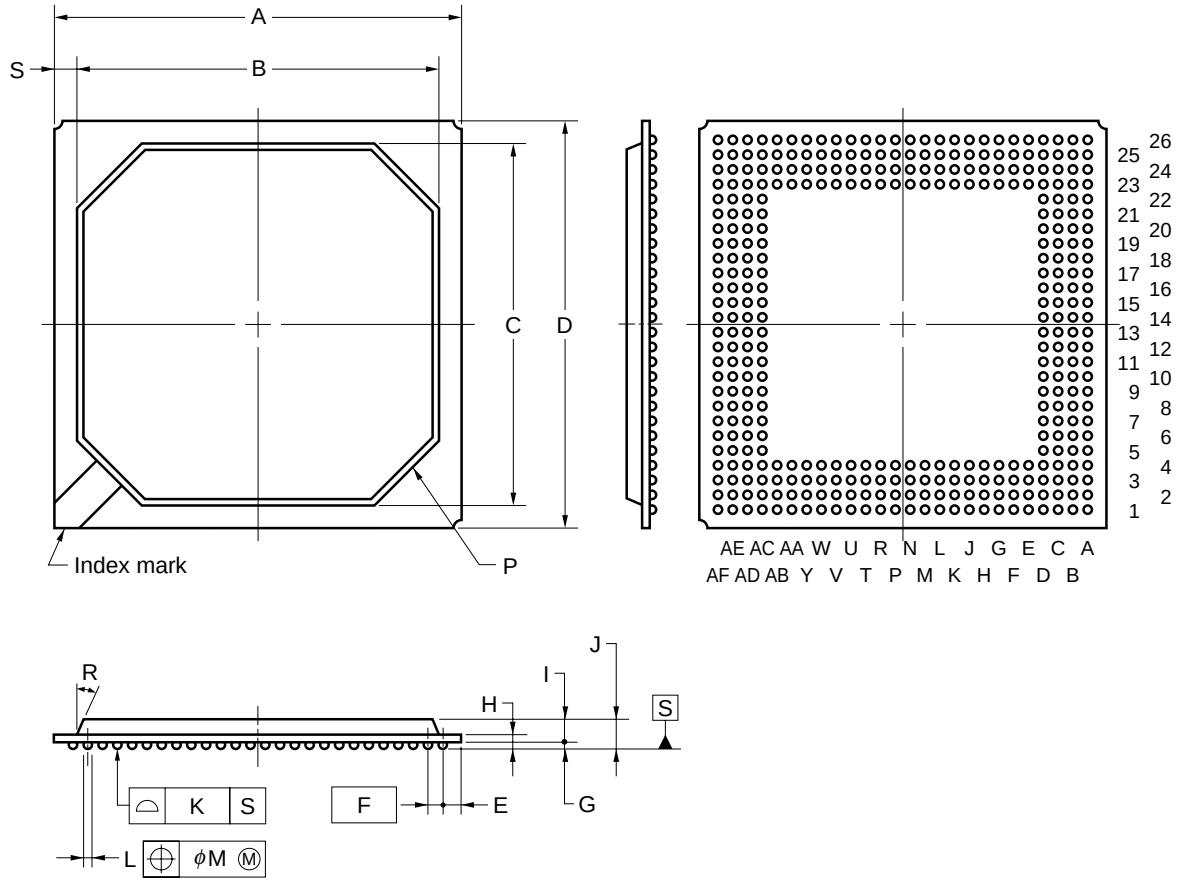
***Figure 2-7: SysAD Bus Timing Parameters***



## 3. Package Drawing

*Figure 3-1: Package Drawing*

### 352-PIN PLASTIC BGA (35x35)




**NOTE**

Each ball centerline is located within ϕ0.3 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|---|---|
| A | 35.0±0.2 |
| B | 30.0 |
| C | 30.0 |
| D | 35.0±0.2 |
| E | 1.62 |
| F | 1.27 (T.P.) |
| G | 0.6±0.1 |
| H | 0.56 |
| I | 1.73±0.15 |
| J | 2.33±0.25 |
| K | 0.15 |
| L | ϕ0.75±0.15 |
| M | 0.3 |
| P | C4.0 |
| R | 30° |
| S | 2.5 |

**S352S1-127-F6-3**

## 4. Recommended Soldering Conditions

Solder this product under the following recommended conditions.
For details of the recommended soldering conditions, refer to information document **Semiconductor Device Mounting Technology Manual (C10535E).**

For soldering methods and conditions other than those recommended, consult NEC.

***Table 4-1: Soldering Conditions***

| Soldering Method | Soldering Condition | Symbol Code of Recommended Soldering Condition |
|---|---|---|
| Infrared reflow | Package peak temperature: 230°C<br>Time of temperature higher than 210°C: 30 seconds max.<br>Number of reflows: 3 max.<br>Number of storage days after opening of dry pack: 3 **Note** | IR30-203-3 |
| VPS | Package peak temperature: 215°C<br>Time of temperature higher than 200°C: 40 seconds max.<br>Number of reflows: 3 max.<br>Number of storage days after opening of dry pack: 3 **Note** | VP15-203-3 |

**Note:** The number of days refers to storage at 25°C, 65% RH MAX after the dry pack has been opened. After that, prebaking is necessary at 125°C for 20 hours (min.), 72 hours (max.).

**Caution: Do not use two or more soldering methods in combination (except partial heating method).**

## 5. Revision History

| Version | Date | Author | Remarks |
|---|---|---|---|
| | | | |
| | | | |
| | | | |
| | | | |

## NOTES FOR CMOS DEVICES

### ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

### ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to $V_{DD}$ or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

### ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
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