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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

Phase-out/Discontinued

MOS INTEGRATED CIRCUIT

μPD30102

VR4102™

64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30102 (VR4102) is one of NEC's VR series RISC (Reduced Instruction Set Computer) microprocessors and is a high-performance 64-/32-bit microprocessor employing the MIPS RISC architecture.

The VR4102 is ideal for applications in battery-driven, high-performance portable information systems. This microprocessor uses the high-performance, super power-saving VR4100™ as the CPU core, and has many peripheral circuits such as DMA controller, software modem interface, serial interface, keyboard interface, IrDA interface, touch panel interface, real-time clock, A/D converter, and D/A converter. Configured with these functions, the VR4102 is suitable for high-speed battery-driven portable information systems. The external memory bus width can be selected between 32 bits and 16 bits, realizing high-speed data transfer.

The functions of the VR4102 are explained in detail in the following manual. Be sure to refer to this manual when designing your system.

- **VR4102 User's Manual (U12739E)**

FEATURES

- Employs 64-bit MIPS architecture
  - Conforms to MIPS III instruction set (deleting FPU, LL, SC instructions)
  - Optimized 5-stage pipeline
- Supports high-speed product-sum operation instructions
- Supports four types of operating modes, enabling more effective power-consumption management
- Internal operating frequency: 54 MHz
- On-chip clock generator
- Address space physical: 32 bits
  virtual : 40 bits
  Integrates 32 double entry TLBs
- High-capacity instruction/data fields separated cache memory
  Instruction field: 4 Kbytes
  Data field : 1 Kbyte
- DRAM interface and mask ROM interface to support flash memory
- 4-channel DMA controller
- Serial interface (NS16550 compatible)
- IrDA controller for infrared-ray communication
- Software modem interface
- A/D and D/A converters to support digital voice I/O
- Supports ISA bus subset
- Power supply voltage: 3.3 V
- Packages: 216-pin plastic LQFP
  224-pin plastic FBGA

APPLICATIONS

- Battery-driven portable information systems
- Embedded controllers, etc.

ORDERING INFORMATION

Part Number	Package
μPD30102GM-54-8EV	216-pin plastic LQFP (fine pitch) (24 × 24 mm)
★ μPD30102S1-54-3C	224-pin plastic FBGA (fine pitch) (16 × 16 mm)

The information in this document is subject to change without notice.

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Printed in Japan

The mark ★ shows major revised points.

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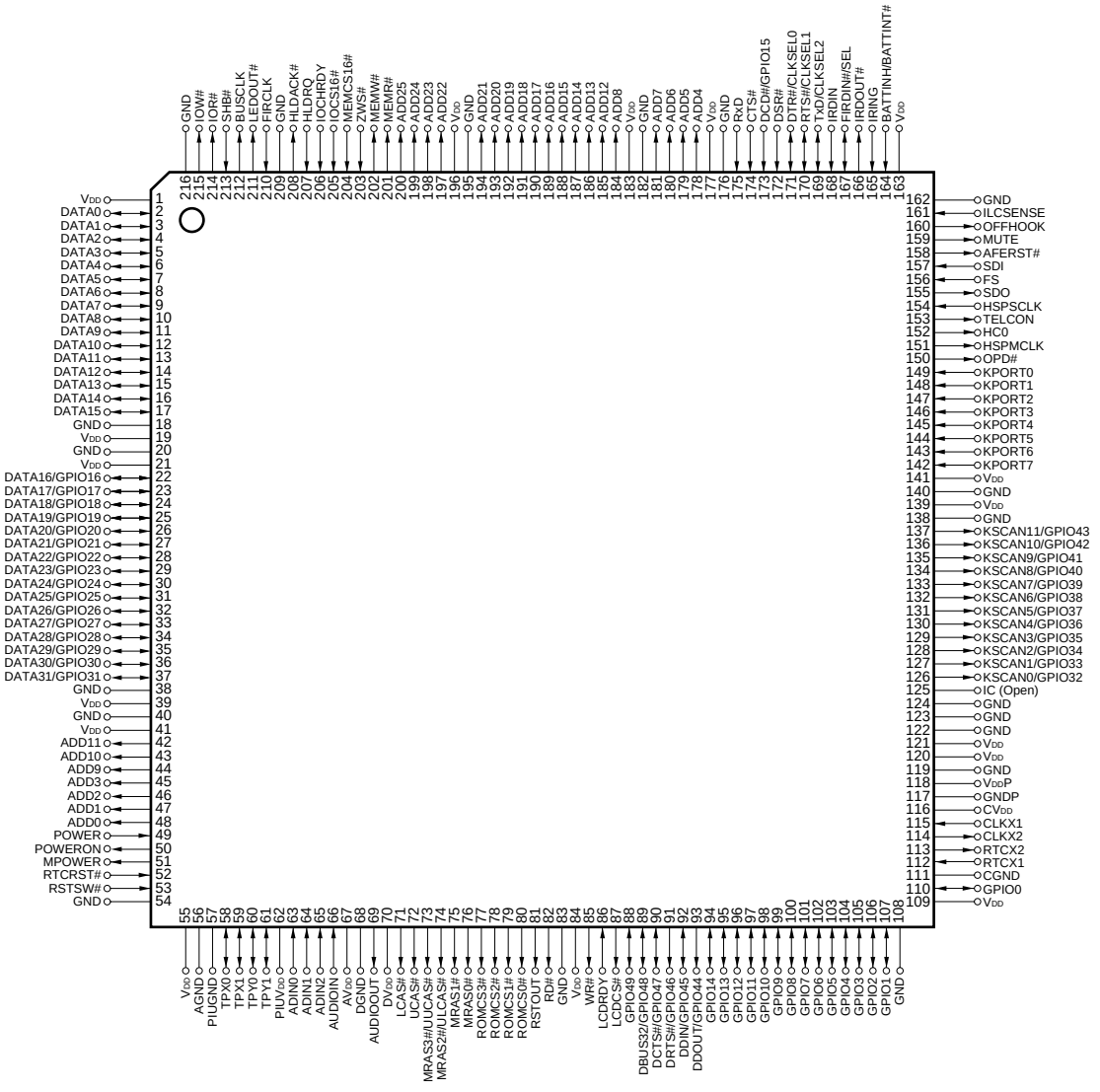
PIN CONFIGURATION

- **216-pin plastic LQFP (24 × 24 mm)**
  μPD30102GM-54-8EV



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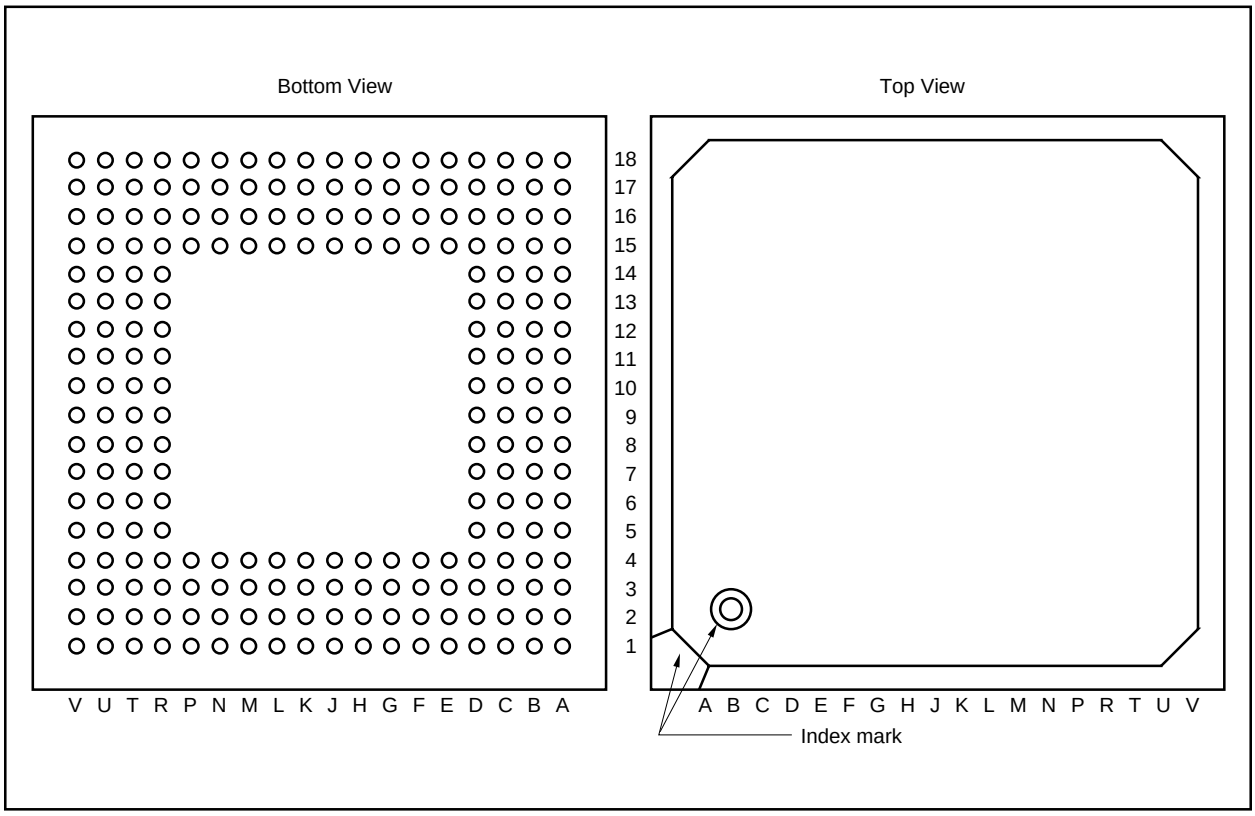
Phase-out/Discontinued

★ • **224-pin plastic FBGA (16 × 16 mm)**
μPD30102S1-54-3C



Phase-out/Discontinued

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	V_{DD}	C15	RTS#/CLKSEL1	H15	GND
A2	SHB#	C16	GND	H16	KPORT6
A3	BUSCLK	C17	ILCSENSE	H17	KPORT4
A4	HLDACK#	C18	AFERST#	H18	V_{DD}
A5	IOCHRDY	D1	DATA5	J1	DATA20/GPIO20
A6	MEMW#	D2	DATA3	J2	DATA17/GPIO17
A7	ADD23	D3	DATA6	J3	DATA22/GPIO22
A8	V_{DD}	D4	GND	J4	DATA19/GPIO19
A9	ADD18	D5	MEMCS16#	J15	KSCAN9/GPIO41
A10	ADD15	D6	ADD25	J16	V_{DD}
A11	ADD8	D7	GND	J17	GND
A12	ADD7	D8	ADD19	J18	KSCAN11/GPIO43
A13	V_{DD}	D9	ADD16	K1	DATA23/GPIO23
A14	DCD#/GPIO15	D10	ADD14	K2	DATA26/GPIO26
A15	TxD/CLKSEL2	D11	V_{DD}	K3	DATA25/GPIO25
A16	IRDOUT#	D12	GND	K4	DATA21/GPIO21
A17	IRING	D13	ADD4	K15	KSCAN7/GPIO39
A18	V_{DD}	D14	CTS#	K16	KSCAN10/GPIO42
B1	DATA1	D15	GND	K17	KSCAN5/GPIO37
B2	IOR#	D16	GND	K18	KSCAN8/GPIO40
B3	IOW#	D17	SDI	L1	DATA27/GPIO27
B4	LEDOUT#	D18	SDO	L2	DATA31/GPIO31
B5	FIRCLK	E1	DATA9	L3	DATA29/GPIO29
B6	HLDRQ#	E2	DATA4	L4	DATA24/GPIO24
B7	ZWS#	E3	DATA7	L15	KSCAN3/GPIO35
B8	ADD24	E4	DATA10	L16	KSCAN6/GPIO38
B9	ADD21	E15	OPD#	L17	KSCAN0/GPIO32
B10	ADD12	E16	HSPSCLK	L18	KSCAN4/GPIO36
B11	ADD6	E17	FS	M1	DATA30/GPIO30
B12	GND	E18	HC0	M2	V_{DD}
B13	DSR#	F1	DATA13	M3	GND
B14	IRDIN	F2	DATA8	M4	DATA28/GPIO28
B15	FIRDIN#/SEL	F3	DATA11	M15	KSCAN2/GPIO34
B16	BATTINH/BATTINT#	F4	DATA14	M16	IC (Open)
B17	OFFHOOK	F15	KPORT3	M17	GND
B18	MUTE	F16	HSPMCLK	M18	KSCAN1/GPIO33
C1	DATA2	F17	TELCON	N1	V_{DD}
C2	DATA0	F18	KPORT1	N2	ADD3
C3	GND	G1	V_{DD}	N3	ADD10
C4	GND	G2	DATA12	N4	GND
C5	GND	G3	DATA15	N15	GND
C6	IOCS16#	G4	GND	N16	V_{DD}
C7	MEMR#	G15	KPORT7	N17	V_{DD}P
C8	ADD22	G16	KPORT2	N18	GND
C9	ADD20	G17	KPORT0	P1	ADD9
C10	ADD17	G18	KPORT5	P2	ADD0
C11	ADD13	H1	DATA16/GPIO16	P3	ADD2
C12	ADD5	H2	GND	P4	ADD11
C13	RxD	H3	DATA18/GPIO18	P15	V_{DD}
C14	DTR#/CLKSEL0	H4	V_{DD}	P16	GNDP

Phase-out/Discontinued

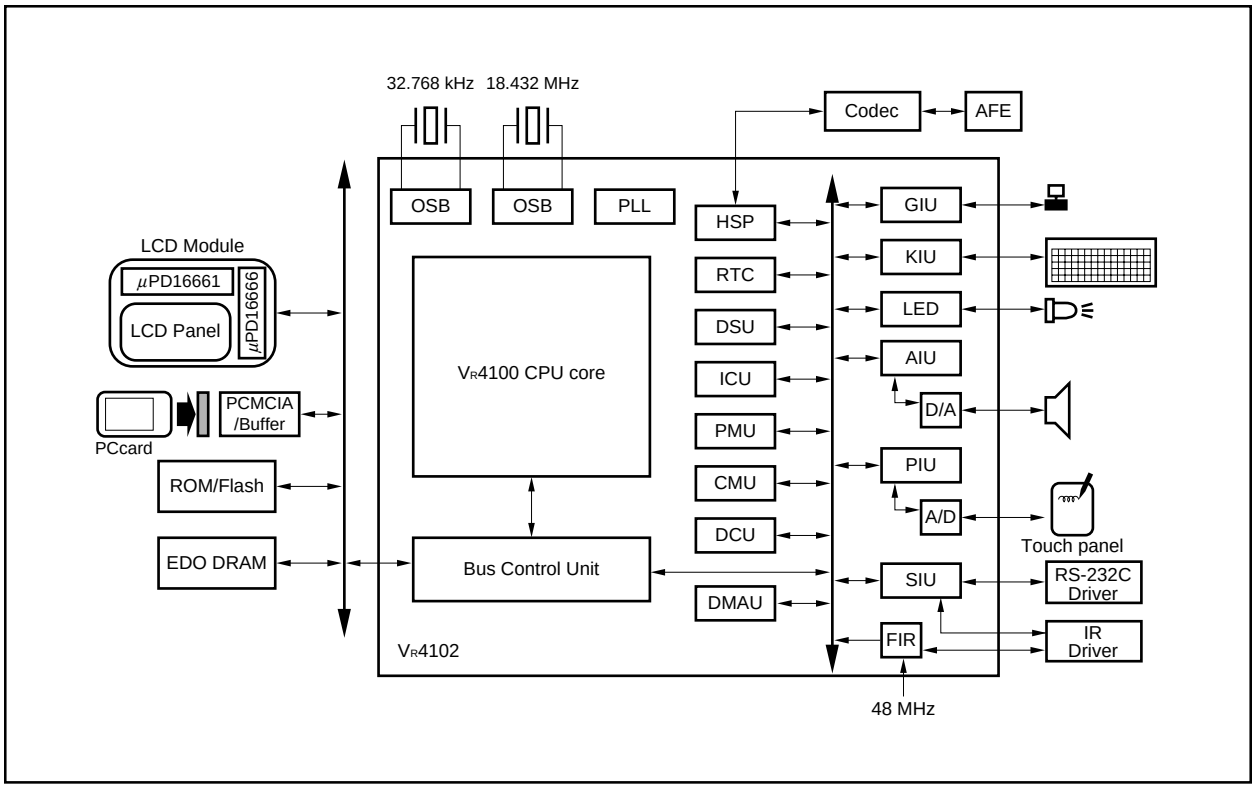
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
P17	CLKX2	T6	AV_{DD}	U13	GPIO9
P18	GND	T7	LCAS#	U14	GPIO6
R1	ADD1	T8	ROMCS2#	U15	GPIO5
R2	POWER	T9	RD#	U16	GPIO1
R3	GND	T10	WR#	U17	GPIO2
R4	GND	T11	DBUS32/GPIO48	U18	CGND
R5	AUDIOIN	T12	DDOUT#/GPIO44	V1	V_{DD}
R6	DV_{DD}	T13	GPIO11	V2	PIUGND
R7	MRAS2#/ULCAS#	T14	GPIO8	V3	TPX0
R8	MRAS1#	T15	GND	V4	TPY1
R9	ROMCS1#	T16	GND	V5	ADIN2
R10	RSTOUT	T17	GPIO0	V6	AUDIOOUT
R11	GND	T18	RTCX1	V7	MRAS3#/UUCAS#
R12	GPIO49	U1	MPOWER	V8	MRAS0#
R13	DDIN/GPIO45	U2	RTCRST#	V9	ROMCS0#
R14	GPIO12	U3	AGND	V10	V_{DD}
R15	GND	U4	TPX1	V11	LCDCS#
R16	CV_{DD}	U5	TPY0	V12	DCTS#/GPIO47
R17	RTCX2	U6	ADIN1	V13	GPIO14
R18	CLKX1	U7	DGND	V14	GPIO10
T1	POWERON	U8	UCAS#	V15	GPIO7
T2	RSTSW#	U9	ROMCS3#	V16	GPIO4
T3	GND	U10	LDCRDY	V17	GPIO3
T4	$PIUV_{DD}$	U11	DRTS#/GPIO46	V18	V_{DD}
T5	ADIN0	U12	GPIO13		

PIN IDENTIFICATION

ADD (0:25) : Address Bus
ADIN (0:2) : General Purpose Input for A/D
AFERST# : AFE Reset
AGND : GND for A/D
AUDIOIN : Audio Input
AUDIOOUT : Audio Output
AV_{DD} : V_{DD} for A/D
BATTINH : Battery Inhibit
BATTINT# : Battery Interrupt Request
BUSCLK : System Bus Clock
CGND : GND for Oscillator
CLKSEL (0:2) : Clock Select
CLKX1 : Clock X1
CLKX2 : Clock X2
CTS# : Clear to Send
CV_{DD} : V_{DD} for Oscillator
DATA (0:31) : Data Bus
DBUS32 : Data Bus 32
DCD# : Data Carrier Detect
DCTS# : Debug Serial Clear to Send
DDIN : Debug Serial Data Input
DDOUT : Debug Serial Data Output
DGND : GND for D/A
DRTS# : Debug Serial Request to Send
DSR# : Data Set Ready
DTR# : Data Terminal Ready
DV_{DD} : V_{DD} for D/A
FIRCLK : FIR Clock
FIRDIN# : FIR Data Input
FS : Frame Synchronization
GND : Ground
GNDP : Ground for PLL
GPIO (0:49) : General Purpose I/O
HC0 : Hardware Control 0
HLDACK# : Hold Acknowledge
HLDRQ# : Hold Request
HSPMCLK : HSP Codec Master Clock
HSPSCLK : HSP Codec Serial Clock
IC : Internally Connected
ILCSENSE : Input Loop Current Sensing
IOCHRDY : I/O Channel Ready
IOCS16# : I/O Chip Select 16
IOR# : I/O Read
IOW# : I/O Write
IRDIN : IrDA Data Input
IRDOUT# : IrDA Data Output
IRING : Input Ring
KPORT (0:7) : Key Code Data Input
KSCAN (0:11) : Key Scan Line
LCAS# : Lower Column Address Strobe
LCDCS# : LCD Chip Select
LCDRDY : LCD Ready
LEDOUT# : LED Output
MEMCS16# : Memory Chip Select 16
MEMR# : Memory Read
MEMW# : Memory Write
MPOWER : Main Power
MRAS(0:3)# : DRAM Row Address Strobe
MUTE : Mute
OFFHOOK : Off Hook
OPD# : Output Power Down
PIUGND : GND for Touch Panel Interface
$PIUV_{DD}$: V_{DD} for Touch Panel Interface
POWER : Power Switch
POWERON : Power On State
RD# : Read
ROMCS(0:3)# : ROM Chip Select
RSTOUT : System Bus Reset Output
RSTSW# : Reset Switch
RTCRST# : Real-time Clock Reset
RTCX1 : Real-time Clock X1
RTCX2 : Real-time Clock X2
RTS# : Request to Send
RxD : Receive Data
SDI : HSP Serial Data Input
SDO : HSP Serial Data Output
SEL : IrDA Module Select
SHB# : System Hi-Byte Enable
TELCON : Telephone Control
TPX (0:1) : Touch Panel X I/O
TPY (0:1) : Touch Panel Y I/O
TxD : Transmit Data
UCAS# : Upper Column Address Strobe
ULCAS# : Lower Byte of Upper Column Address Strobe
UUCAS# : Upper Byte of Upper Column Address Strobe
V_{DD} : Power Supply Voltage
$V_{DD}P$: VDD for PLL
WR# : Write
ZWS# : Zero Wait State

Remark # indicates active low.

INTERNAL BLOCK DIAGRAM AND EXAMPLE OF CONNECTION OF EXTERNAL BLOCKS



CPU CORE INTERNAL BLOCK DIAGRAM

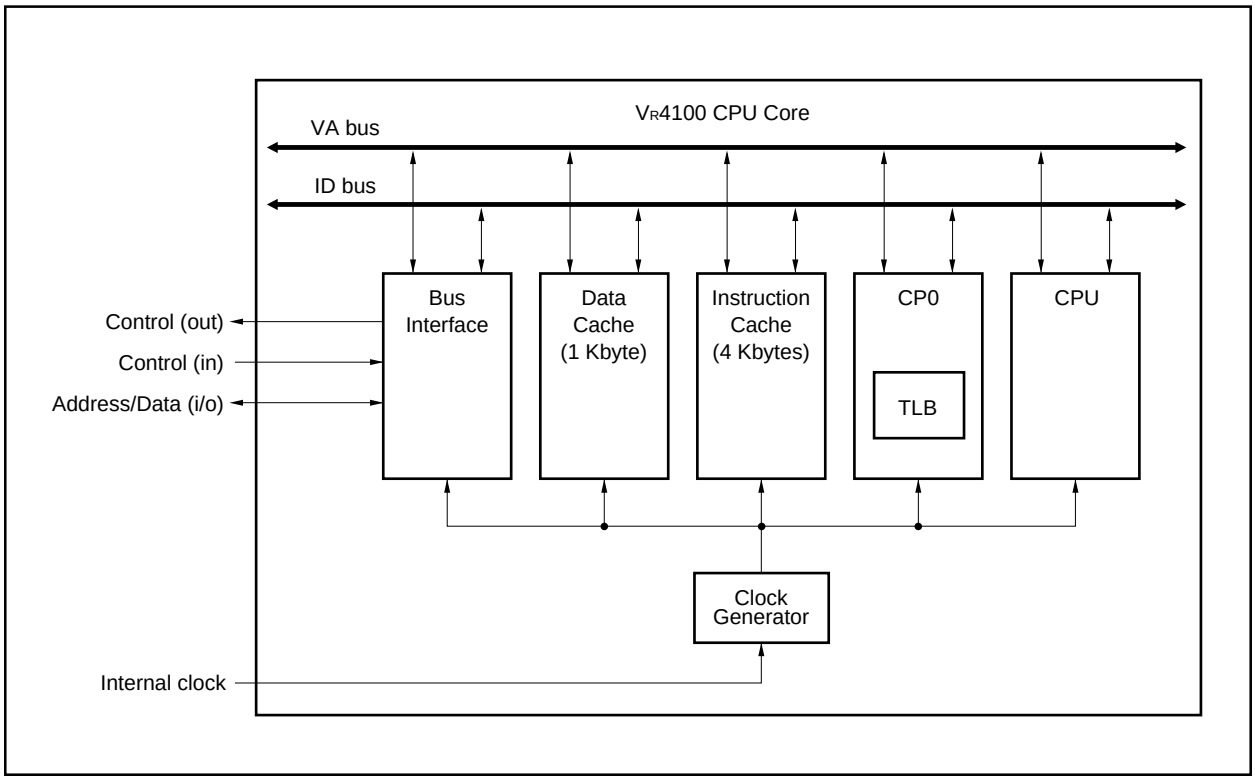


TABLE OF CONTENTS

1. PIN FUNCTIONS

Remark # indicates active low.

1.1 Pin Functions

(1) System bus interface signals (1/2)

Signal Name	I/O	Function
ADD (0:25)	O	This is a 25-bit address bus. Used to specify addresses of the VR4102, DRAM, ROM, LCD, and system bus (ISA).
DATA (0:15)	I/O	This is a 16-bit data bus. Used to transfer data from the VR4102 to DRAM, ROM, LCD, and system bus, and vice versa.
DATA (16:31)/ GPIO (16:31)	I/O	This function differs depending on how the DBUS32 pin is set. <When DBUS32 = 1> It is the high-order 16 bits of the 32-bit data bus. This bus is used for transmitting and receiving data between the VR4102 and the DRAM and ROM. <When DBUS32 = 0> It is a general-purpose I/O (GPIO) port.
LCDCS#	O	This is the LCD chip select signal. This signal is active when the VR4102 is performing LCD access using the ADD/DATA bus.
RD#	O	Active when the VR4102 is reading data from the LCD, RAM, or ROM.
WR#	O	Active when the VR4102 is writing data to the LCD, RAM, or ROM.
LCDRDY	I	This is the LCD ready signal. Set this signal as active when the LCD controller is ready to be accessed from the VR4102.
ROMCS (0:3)#	O	This is the ROM chip select signal. It is used to select a ROM to be accessed from among up to four connected ROM units.
UUCAS#/ MRAS3#	O	This function differs depending on how the DBUS32 pin is set. <When DBUS32 = 1> UUCAS# This signal is active when a valid column address is output via the ADD bus during access of DATA (24:31) in the 32-bit data bus. <When DBUS32 = 0> MRAS3# This is the DRAM's RAS signal. Up to four DRAM units can be connected, and this signal is active when a valid row address is output via the ADD bus for the DRAM connected to the high-order address.
ULCAS#/ MRAS2#	O	This function differs depending on how the DBUS32 pin is set. <When DBUS32 = 1> ULCAS# This signal is active when a valid column address is output via the ADD bus during access of DATA (16:23) in the 32-bit data bus. <When DBUS32 = 0> MRAS2# This is the DRAM's RAS signal. This signal is active when a valid row address is output via the ADD bus for the DRAM connected to the next-highest address after the highest high-order address.
MRAS (0:1)#	O	This is the DRAM's RAS-only signal.
UCAS#	O	This is the DRAM's CAS signal. This signal is active when a valid column address is output via the ADD bus during access of DATA (8:15) in the DRAM.

(2/2)

Signal Name	I/O	Function
LCAS#	O	This is the DRAM's CAS signal. This signal is active when a valid column address is output via the ADD bus during access of DATA (0:7) in the DRAM.
BUSCLK	O	This is the system bus clock. It is used to output the clock that is supplied to the controller on the system bus. The frequency to be output is determined according to the state of pins CLKSEL2/TxD, CLKSEL1/RTS#, and CLKSEL0/DTR#. (See **(5) RS-232C interface signals**)
SHB#	O	This is the system bus high-byte enable signal. During system bus access, this signal is active when the high-order byte is valid on the data bus.
IOR#	O	This is the system bus I/O read signal. It is active when the VR4102 accesses the system bus to read data from an I/O port.
IOW#	O	This is the system bus I/O write signal. It is active when the VR4102 accesses the system bus to write data to an I/O port.
MEMR#	O	This is the system bus memory read signal. It is active when the VR4102 accesses the system bus to read data from memory.
MEMW#	O	This is the system bus memory write signal. It is active when the VR4102 accesses the system bus to write data to memory.
ZWS#	I	This is the system bus zero wait state signal. Set this signal as active to enable the controller on the system bus to be accessed by the VR4102 without a wait interval.
RSTOUT	O	This is the system bus reset signal. It is active when the VR4102 resets the system bus controller.
MEMCS16#	I	This is a dynamic bus sizing request signal. Set this signal as active when system bus memory accesses data in 16-bit width (however, the DRAM bus memory space that is controlled by the DBUS32 pin is excepted).
IOCS16#	I	This is a dynamic bus sizing request signal. Set this signal as active when system bus I/O accesses data in 16-bit width.
IOCHRDY	I	This is the system bus ready signal. Set this signal as active when the system bus controller is ready to be accessed by the VR4102.
HLDRQ#	I	This is a hold request signal for the system bus and DRAM bus that is sent from an external bus master.
HLDACK#	O	This is a hold acknowledge signal for the system bus and DRAM bus that is sent to an external bus master.
DBUS32/GPIO48	I/O	This function differs depending on how the RTCRST# pin is set. <When RTCRST# = 1> This can be used as a general-purpose output port. <When RTCRST# = 0> This can be used as the data-bus width switch signal. The data is sampled while the RTCRST# signal is low, and is retained while the RTCRST3 signal is high. 1: Data bus is used in 32-bit width 0: Data bus is used in 16-bit width

(2) Clock interface signals

Signal Name	I/O	Functional Description
RTCX1	I	This is the 32.768-kHz oscillator's input pin for RTC. It is connected to one side of a crystal resonator.
RTCX2	O	This is the 32.768-kHz oscillator's output pin for RTC. It is connected to one side of a crystal resonator.
CLKX1	I	This is the 18.432-MHz oscillator's input pin for the CPU core and peripheral units. It is connected to one side of a crystal resonator.
CLKX2	O	This is the 18.432-MHz oscillator's output pin for the CPU core and peripheral units. It is connected to one side of a crystal resonator.
FIRCLK	I	This is the 48-MHz clock input pin for FIR. Fix this at high level when FIR is not used.

(3) Battery monitor interface signals

Signal Name	I/O	Function
BATTINH/ BATTINT#	I	This function differs depending on how the MPOWER pin is set. <When MPOWER = 0> BATTINH function This is an interrupt signal that is output when remaining power is low while battery is ON. The external agent checks the remaining battery power and asserts the signal at this pin if the supplied voltage is sufficient for current operations. 1 : Battery OK 0 : Battery low <When MPOWER = 1> BATTINT# function This is an interrupt signal that is output when remaining power is low during normal operations. The external agent checks the remaining battery power and asserts the signal at this pin if voltage sufficient for operations cannot be supplied.

(4) Initialization interface signals

Signal Name	I/O	Functional Description
MPOWER	O	Signal to turn ON main power. V_R4102 turns ON power supply to external DC/DC converter by asserting this pin active.
POWERON	O	Signal indicating that V_R4102 is to start activation. It is asserted active when start cause is detected, and deasserted inactive after battery check has been completed.
POWER	I	Signal indicating that power-ON switch has been pressed. When power-ON switch has been pressed, external circuit asserts this pin active.
RSTSW#	I	Signal indicating that reset switch has been pressed. When reset switch has been pressed, external circuit asserts this pin active.
RTCRST#	I	Signal resetting RTC. When power is supplied to system for first time, external circuit asserts this pin active for 600 ms.

(5) RS-232C interface signals

Signal Name	I/O	Function
RxD	I	This is a receive data signal. It is used when an external device sends serial data to the VR4102.
CTS#	I	This is the transmit enable ("clear-to-send") signal. This signal is asserted when the RS-232C controller is ready to receive transmission of serial data.
DCD#/ GPIO15	I	This is a carrier detection signal. Assert this signal active when valid serial data is being received. It is also used when detecting a power-on factor for the VR4102. When this is not used as the DCD# signal, this can be used as an interrupt detection I/O signal for the GIU unit.
DSR#	I	This is the data set ready signal. Assert this signal active to set up transmission and reception of serial data between the RS-232C controller and the VR4102.
TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0	I/O	This function differs depending on the state of the RTCRST# signal. <When RTCRST# = 1> These signals are used to perform serial communication. TxD/CLKSEL2 signal: This is a transmit data signal. It is used when the VR4102 sends serial data to an external device. RTS#/CLKSEL1 signal: This is a transmit request signal. This signal is asserted when the VR4102 is ready to receive serial data from the RS-232C controller. DTR#/CLKSEL0 signal: This is a terminal equipment ready signal. This signal is asserted when the VR4102 is ready to transmit or receive serial data. <When RTCRST# = 0> These signals (CLKSEL (0:2)) are used to set the operating frequency of the CPU core and the BUSCLK output frequency.

★

CLKSEL[2:0]	CPU core operating frequency (MHz)	BUSCLK output frequency (MHz)
111	RFU	
110	RFU	
101	53.6	6.700
100	49.2	6.075
011	45.4	5.675
010	42.1	5.275

Caution The selection of some frequencies shown above may be disabled in the future.

(6) IrDA interface signals

Signal Name	I/O	Function
IRDIN	I	This is the IrDA serial data input signal. It is used when the IrDA controller sends the serial data to the VR4102. Both FIR and SIR can be used. However, if the IrDA controller used is made by HP, this signal should be used only for SIR.
FIRDIN#/SEL	I/O	This function differs according to the IrDA controller used. To switch the controller to be used, see **Chapter 15 SIU**. <When an HP's controller is used> FIRDIN#: FIR receive data input signal <When a TEMIC's controller is used> SEL: FIR/SIR switch signal output signal <When a SHARP's controller is used> Usage is prohibited.
IRDOUT#	O	This is the IrDA serial data output signal. It is used when the VR4102 sends serial data to the IrDA controller.

(7) Debug serial interface signals

Signal Name	I/O	Function
DDOUT/GPIO44	O	This is the debug serial data output signal. It is used when the VR4102 sends serial data to an external device. When this pin is not used as the DDOUT signal, it can be used as a general-purpose output port.
DDIN/GPIO45	I/O	This is the debug serial data input signal. It is used when an external device sends serial data to the VR4102. When this pin is not used as the DDIN signal, it can be used as a general-purpose output port.
DRTS#/GPIO46	O	This is a transmission request signal. The VR4102 asserts this signal before sending serial data. When this pin is not used as the DRTS# signal, it can be used as a general-purpose output port.
DCTS#/GPIO47	I/O	This is a transmit acknowledge signal. The VR4102 asserts this signal when it is ready to receive transmitted serial data. When this pin is not used as the DCTS# signal, it can be used as a general-purpose output port.

(8) Keyboard interface signals

Signal Name	I/O	Function
KPORT (0:7)	I	This is a keyboard scan data input signal. It is used to scan for pressed keys on the keyboard.
KSCAN (0:11)/ GPIO (32:43)	O	These signals are used as keyboard scan data output signals and a general-purpose output port. The scan line is set as active when scanning for pressed keys on the keyboard. Pins that are not used for the key scan operation can be used as a general-purpose output port.

(9) Audio interface signals

Signal Name	I/O	Function
AUDIOIN	I	This is an audio input signal.
AUDIOOUT	O	This is an audio output signal. Analog signals that have been converted via the on-chip 10-bit D/A converter are output.

(10) Touch panel interface signals

Signal Name	I/O	Function
TPX (0:1)	I/O	This is an I/O signal that is used for the touch panel. It uses the voltage applied to the X coordinate and the voltage input to the Y coordinate to detect which coordinates on the touch panel are being pressed.
TPY (0:1)	I/O	This is an I/O signal that is used for the touch panel. It uses the voltage applied to the Y coordinate and the voltage input to the X coordinate to detect which coordinates on the touch panel are being pressed.
ADIN (0:2)	I	This is a general-purpose A/D input signal.

(11) General-purpose I/O signals

Signal Name	I/O	Function
GPIO (0:3)	I/O	These are maskable activation factor input signals. After start-up, they are used as ordinary GPIO pins.
GPIO (4:8)	I/O	These are general-purpose I/O pins.
★ GPIO (9:12)	I/O	These are maskable activation factor input signals. After start-up, they are used as ordinary GPIO pins.
GPIO (13:14)	I/O	These are general-purpose I/O pins.
GPIO15/DCD#	I	See **(5) RS-232C interface signals** in this section.
GPIO (16:31)/ DATA (16:31)	I/O	See **(1) System bus interface signals** in this section.
GPIO (32:43)/ KSCAN (0:11)	O	See **(8) Keyboard interface signals** in this section.
GPIO44/DDOUT	O	See **(7) Debug serial interface signals** in this section.
GPIO45/DDIN	I/O	See **(7) Debug serial interface signals** in this section.
GPIO46/DRTS#	O	See **(7) Debug serial interface signals** in this section.
GPIO47/DCTS#	I/O	See **(7) Debug serial interface signals** in this section.
GPIO48/DBUS32	I/O	See **(1) System bus interface signals** in this section.
GPIO49	O	This function differs depending on the state of the RTCRST# signal. <When RTCRST# = 1> It can be used as a general-purpose output port. <When RTCRST# = 0> Set to the low level.

(12) HSP modem interface signals

Signal Name	I/O	Function
IRING	I	This signal is asserted active when detecting the RING signal.
ILCSENSE	I	Handset detect signal
OFFHOOK	O	On-hook relay control signal
MUTE	O	Modem speaker mute control signal
AFERST#	O	CODEC reset signal
SDI	I	Serial input signal from CODEC
FS	I	Frame synchronization signal from CODEC
SDO	O	Serial output signal to CODEC
HSPSCLK	I	Operation clock input of modem interface block for CODEC
TELCON	O	Handset relay control signal
HS0	O	CODEC control signal
HSPMCLK	O	Clock output to CODEC
OPD#	O	This signal is asserted active when the power supply of CODEC or DAA is ON.

(13) LED interface signal

Signal Name	I/O	Function
LEDOUT#	O	This is an output signal for lighting LEDs.

(14) Dedicated VDD and GND signals

Signal Name	Function
$V_{DD}P$	This is the dedicated V_{DD} for the PLL unit.
GNDP	This is the dedicated GND for the PLL unit.
CV_{DD}	This is the dedicated V_{DD} for the oscillator.
CGND	This is the dedicated GND for the oscillator.
DV_{DD}	This is the dedicated V_{DD} for the D/A converter. The voltage applied to this pin becomes the maximum value for AUDIOOUT's analog output.
DGND	This is the dedicated GND for the D/A converter. The voltage applied to this pin becomes the minimum value for AUDIOOUT's analog output.
AV_{DD}	This is the dedicated V_{DD} for the A/D converter. The voltage applied to this pin becomes the maximum voltage value for the AD interface signal.
AGND	This is the dedicated GND for the A/D converter. The voltage applied to this pin becomes the minimum voltage value detectable by the AD interface signals.
$PIUV_{DD}$	This is the dedicated V_{DD} for the touch panel interface.
PIUGND	This is the dedicated GND for the touch panel interface.

1.2 Pin Status in Specific Status

(1/3)

Signal Name	After Reset by RTCRST	After Reset Deadman's SW or by RSTSW	During Suspend Mode	In Hibernate Mode or on Shutdown by HAL Timer	During Bus Hold	Internal Process	External Process	Drivability
ADD (0:25)	0	0	**Note 1**	0	Hi-Z	—	—	120 pF
DATA (0:15)	0	0	**Note 1**	0	Hi-Z	—	—	40 pF
DATA (16:31)/ GPIO (16:31)	0/ Hi-Z	0/ Hi-Z	**Note 1**	0/ Hi-Z	Hi-Z/ **Note 1**	—	—/ pull-up/ pull-down	40 pF
LCDCS#	Hi-Z	1	1	Hi-Z	1	—	—	40 pF
RD#	Hi-Z	1	1	Hi-Z	Hi-Z	—	**Note 2**	120 pF
WR#	Hi-Z	1	1	Hi-Z	Hi-Z	—	**Note 2**	120 pF
LCDRDY	—	—	—	—	—	—	Pull-up	—
ROMCS (0:3)#	Hi-Z	1	1	Hi-Z	1	—	—	40 pF
UUCAS#/MRAS3#	1	**Note 3**	0	0	Hi-Z	—	**Note 2**	40 pF
UUCAS#/MRAS2#	1	**Note 3**	0	0	Hi-Z	—	**Note 2**	40 pF
MRAS (0:1)#	1	**Note 3**	0	0	Hi-Z	—	**Note 2**	40 pF
UCAS#	1	**Note 3**	0	0	Hi-Z	—	**Note 2**	40 pF
LCAS#	1	**Note 3**	0	0	Hi-Z	—	**Note 2**	40 pF
BUSCLK	0	0	0	0	**Note 4**	—	—	40 pF
SHB#	Hi-Z	1	1	Hi-Z	Hi-Z	—	**Note 2**	40 pF
IOR#	Hi-Z	1	1	Hi-Z	Hi-Z	—	**Note 2**	40 pF
IOW#	Hi-Z	1	1	Hi-Z	Hi-Z	—	**Note 2**	40 pF
MEMR#	Hi-Z	1	1	Hi-Z	Hi-Z	—	**Note 2**	40 pF
MEMW#	Hi-Z	1	1	Hi-Z	Hi-Z	—	**Note 2**	40 pF
ZWS#	—	—	—	—	—	**Note 5**	Pull-up	—
RSTOUT	Hi-Z	1	0	Hi-Z	**Note 6**	—	Pull-up	40pF
IOCS16#	—	—	—	—	—	**Note 5**	Pull-up	—
MEMCS16#	—	—	—	—	—	**Note 5**	Pull-up	—
IOCHRDY	—	—	—	—	—	**Note 5**	Pull-up	—

Notes 1. The previous "Full Speed Mode" state is retained.

2. When using the bus hold function, be sure to pull up this pin.

3. Reset by RSTSW# signal: This pin outputs low level (self-refresh function).
Reset by deadman's switch: This pin outputs high level.

4. Bus hold from suspend mode: Outputs low level.
Bus hold from full speed mode or standby mode: Outputs clocks.

5. Intermediate-level input is enabled when the MPOWER pin is set for low-level output.

6. Normal operation is performed.

Remarks 0: Low-level output, 1: High-level output, Hi-Z: High impedance

(2/3)

Signal Name	After Reset by RTCRST	After Reset Deadman's SW or by RSTSW	During Suspend Mode	In Hibernate Mode or on Shutdown by HAL Timer	During Bus Hold	Internal Process	External Process	Drivability
HIDREQ#	—	—	—	—	—	**Note 1**	**Note 2**	—
HLDACK#	Hi-Z	1	**Note 3**	Hi-Z	**Note 3**	—	—	40 pF
RTCX1	—	—	—	—	—	—	Oscillator	—
RTCX2	—	—	—	—	—	—	Oscillator	—
CLKX1	—	—	—	—	—	—	Oscillator	—
CLKX2	—	—	—	—	—	—	Oscillator	—
FIRCLK	—	—	—	—	—	—	**Note 4**	—
BATTINH/ BATTINT#	—	—	—	—	—	Schmitt-triggered input	—	—
MPOWER	0	1	1	0	1	—	—	40 pF
POWERON	0	0	0	0	0	—	—	40 pF
POWER	—	—	—	—	—	Schmitt-triggered input	—	—
RSTSW#	—	—	—	—	—	Schmitt-triggered input	—	—
RTCRST#	—	—	—	—	—	Schmitt-triggered input	—	—
RxD	—	—	—	—	—	—	—	—
TxD/CLKSEL2	Hi-Z	1	1	1	**Note 3**	—	Pull-up/ pull-down	40 pF
RTS#/CLKSEL1	Hi-Z	1	1	1	**Note 3**	—	Pull-up/ pull-down	40 pF
CTS#	—	—	—	—	—	—	—	—
DCD#/GPIO15	—	—	—	—	—	—	Pull-up	—
DTR#/CLKSEL0	Hi-Z	1	1	1	**Note 3**	—	Pull-up/ pull-down	40 pF
DSR#	—	—	—	—	—	—	—	—
IRDIN	—	—	—	—	—	—	Pull-up	—
IRDOUT#	0	0	0	0	**Note 3**	—	—	40 pF
FIRDIN#/SEL	Hi-Z	Hi-Z	**Note 5**	Hi-Z	**Note 5**	—	Pull-up/ pull-down	40 pF
DDIN/ GPIO45**Note 6**	Hi-Z/ Hi-Z	Hi-Z/ Hi-Z	Hi-Z/ **Note 5**	Hi-Z/ Hi-Z	Hi-Z/ **Note 5**	—	—	40 pF
DDOUT/ GPIO44**Note 6**	1	1	1	1	1	—	—	40 pF
DRTS#/ GPIO46**Note 6**	1	1	1	1	1	—	—	40 pF
DCTS#/ GPIO47**Note 6**	Hi-Z/ Hi-Z	Hi-Z/ Hi-Z	Hi-Z/ **Note 5**	Hi-Z/ Hi-Z	Hi-Z/ **Note 5**	—	—	40 pF

Notes 1. The previous "Full Speed Mode" state is retained.

2. When using the bus hold function, be sure to pull up this pin.

3. Reset by RSTSW# signal: This pin outputs low level (self-refresh function).
Reset by deadman's switch: This pin outputs high level.

4. Bus hold from suspend mode: Outputs low level.
Bus hold from full speed mode or standby mode: Outputs clocks.

5. Intermediate-level input is enabled when the MPOWER pin is set for low-level output.

6. Normal operation is performed.

Remarks 0: Low-level output, 1: High-level output, Hi-Z: High impedance

(3/3)

Signal Name	After Reset by RTCRST	After Reset Deadman's SW or by RSTSW	During Suspend Mode	In Hibernate Mode or on Shutdown by HAL Timer	During Bus Hold	Internal Process	External Process	Drivability
KPORT (0:7)	—	—	—	—	—	Pull-up/ down	—	—
KSCAN (0:11)/ GPIO (32:43)Note 1	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 3**	—	—	40 pF
AUDIOOUT	0	0	**Note 2**	0	**Note 3**	—	**Note 4**	—
TPX (0:1)	Hi-Z	1	**Note 2**	1	**Note 3**	—	—	120 pF or higher
TPY (0:1)	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 3**	—	—	120 pF or higher
ADIN (0:1)	—	—	—	—	—	—	—	—
AUDIOIN	—	—	—	—	—	—	—	—
GPIO (5:14)	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 3**	—	Pull-up/ down	40 pF
GPIO (0:4)	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 3**	Schmitt-triggered input	Pull-up/ down	40 pF
IRING	—	—	—	—	—	Schmitt-triggered input	Pull-down	—
ILCSENSE	—	—	—	—	—	—	Pull-down	—
OFFHOOKNote 5	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**	—	—	40 pF
MUTENote 5	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**	—	—	40 pF
AFERST#Note 5	0	0	**Note 2**	0	**Note 2**	—	—	40 pF
SDI	—	—	—	—	—	—	Pull-up/ down	—
FS	—	—	—	—	—	—	Pull-up/ down	—
SDO	0	0	**Note 2**	0	**Note 2**	—	—	40 pF
HSPSCLK	—	—	—	—	—	—	—	—
TELCONNote 5	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**	—	—	40 pF
HC0Note 5	0	0	**Note 2**	0	**Note 2**	—	—	40 pF
HSPMCLKNote 5	0	0	**Note 2**	0	**Note 2**	—	—	40 pF
OPD#	0	0	**Note 2**	0	**Note 2**	—	—	40 pF
LEDOUT#	1	**Note 3**	**Note 3**	**Note 3**	**Note 3**	—	—	40 pF
DBUS32/ GPIO48Note 6	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**	—	Pull-up/ down	40 pF
GPIO49Note 6	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**	—	Pull-down	—

Notes 1. The previous "Full Speed Mode" state is retained.

2. When using the bus hold function, be sure to pull up this pin.

3. Reset by RSTSW# signal: This pin outputs low level (self-refresh function).
Reset by deadman's switch: This pin outputs high level.

4. Bus hold from suspend mode: Outputs low level.
Bus hold from full speed mode or standby mode: Outputs clocks.

5. Intermediate-level input is enabled when the MPOWER pin is set for low-level output.

6. Normal operation is performed.

Remarks 0: Low-level output, 1: High-level output, Hi-Z: High impedance

2. INTERNAL BLOCKS

For the internal block configuration, see the figure in P. 4.

2.1 VR4100 CPU Core

(1) CPU

The CPU processes integer instructions and consists of 64-bit register files, a 64-bit integer data bus, and a sum-of-products operation unit.

(2) Coprocessor 0 (CP0)

The CP0 has a memory management unit (MMU) and an exception processing function. The MMU translates addresses and checks whether an access is made between different types (user, supervisor, or kernel) of memory segments. Translation of virtual addresses to physical addresses is performed by TLB (high-speed translation lookaside buffer).

(3) Instruction cache

The instruction cache is 4-Kbyte capacity, consisting of direct mapping, virtual index, and physical tag type.

(4) Data cache

The data cache is 1-Kbyte capacity, consisting of direct mapping, virtual index, physical tag, and write back type.

(5) CPU bus interface

The CPU bus interface controls data transfer between the VR4100 CPU core and BCU, one of the peripheral units. As the bus interface for the VR4100 CPU core, two 32-bit address/data multiplexed buses each for input and output, clock signals, and interrupt control signals are used.

2.2 Clock Generator

The following clock inputs are oscillated to generate and supply clocks to internal units.

- 32.768-kHz clock for RTC. The 32.768-kHz clock generated by the crystal resonator is oscillated by the internal oscillator, and supplied to the RTC unit.
- 18.432-MHz clock for serial interface, touch panel interface, and reference operating clock of the VR4102. The 18.432-MHz clock generated by the crystal resonator is oscillated by the internal oscillator, multiplied by PLL (phase-locked loop), to generate the pipeline clock (PClock). The internal bus clock (TClock) is generated from PClock.

2.3 BCU (Bus Control Unit)

The BCU internally transfers data with the VR4100 CPU core via SysAD bus (internal). It also controls the LCD controller, DRAM, ROM (flash memory or mask ROM), and PCMCIA controller connected to the system bus, and transfers data with the above devices via ADD and DATA buses.

2.4 RTC (Real-time Clock)

The RTC has a precise counter that operates with a 32.768-kHz clock supplied from the clock generator. It also has several counters and compare registers for various interrupts.

2.5 DSU (Deadman's Switch Unit)

The DSU is used to check whether the processor is operating normally. If the software does not clear the register of this unit at specific intervals, the system is shut down.

2.6 ICU (Interrupt Control Unit)

The ICU controls interrupt requests generated from the external and internal sources of the VR4102, and reports an interrupt request, if any, to the VR4100 CPU core.

2.7 PMU (Power Management Unit)

The PMU outputs signals necessary for controlling the power of the entire system, including the VR4102. It also controls the PLL of the VR4100 CPU core and the internal clocks (PClock, TClock, and MasterOut) in the power-saving mode.

2.8 DMAAU (Direct Memory Access Address Unit)

The DMAAU controls three types of DMA transfer addresses.

2.9 DCU (Direct Memory Access Control Unit)

The DCU controls addresses of three types of DMA transfers.

2.10 CMU (Clock Mask Unit)

The CMU controls supply of the clocks (TClock or MasterOut) from the VR4100 CPU core to the internal peripheral units.

2.11 GIU (General Purpose I/O Unit)

GIU controls fifty GPIO pins.

2.12 AIU (Audio Interface Unit)

AIU performs mic-input sampling and audio-signal output by controlling the internal A/D and D/A converters.

2.13 KIU (Keyboard Interface Unit)

The KIU has 8/10/12 scan lines and eight detection lines to detect input of 64/80/96 keys. It can also detect roll over of 2 or 3 keys by adding diodes.

2.14 PIU (Touch Panel Interface Unit)

PIU performs touch detection of touch panel by controlling the internal A/D converter.

2.15 DSIU (Debug Serial Interface Unit)

The DIU is a serial interface for debugging and supports a transfer rate of up to 115 kbps.

2.16 SIU (Serial Interface Unit)

The SIU is a serial interface that is compatible with NS 16550 and is conforming to the RS-232C Standards, and supports a transfer rate of up to 115 kbps. In addition, an IrDA serial interface that supports a transfer rate of 115 kbps is also included, though this IrDA serial interface is exclusively used with the RS-232C interface.

Phase-out/Discontinued

2.17 FIR (Fast IrDA Unit)

The FIR unit is a unit to perform IrDA communication of 0.576 Mbps through 4 Mbps. This unit operates with the dedicated 48-MHz clock input.

2.18 HSP (Host Signal Processing Unit)

The HSP unit is a unit to realize a software modem.

2.19 LED (LED Unit)

The LED unit is a unit to control lighting of external LEDs.

3. INTERNAL ARCHITECTURE

3.1 Pipeline

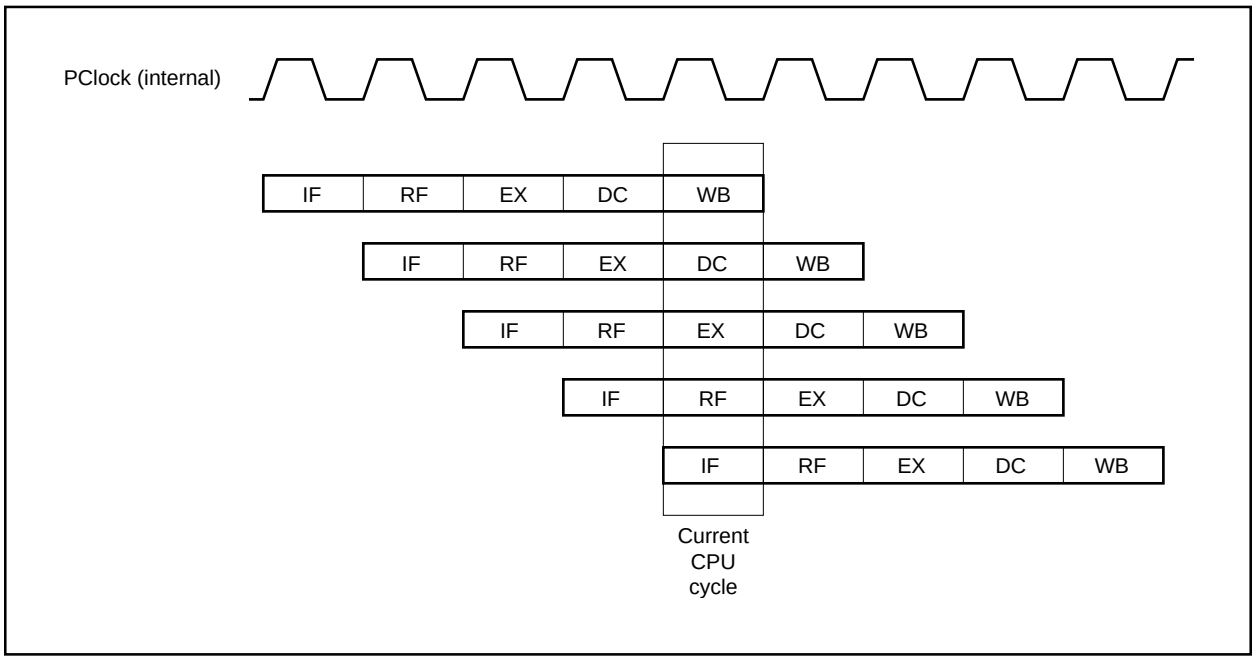
Each instruction is executed in the following five steps:

(1) IF Instruction fetch
(2) RF Register fetch
(3) EX Execution
(4) DC Data cache fetch
(5) WB Write back

The VR4102 has a five-stage pipeline. It takes five clocks to execute each instruction, but instructions can be executed in parallel. The pipeline clock, PClock, is determined by the setting of the CLKSEL (0:2) pins.

The following figure outlines the pipeline.

Figure 3-1. Pipeline of VR4102 (5-stage)



3.2 CPU Registers

Figure 3-2 shows the CPU registers of the VR4102. The bit width of these registers is determined by the operation mode of the processor (32 bits in 32-bit mode or 64 bits in 64-bit mode).

Of the 32 general-purpose registers, the following two have a special meaning.

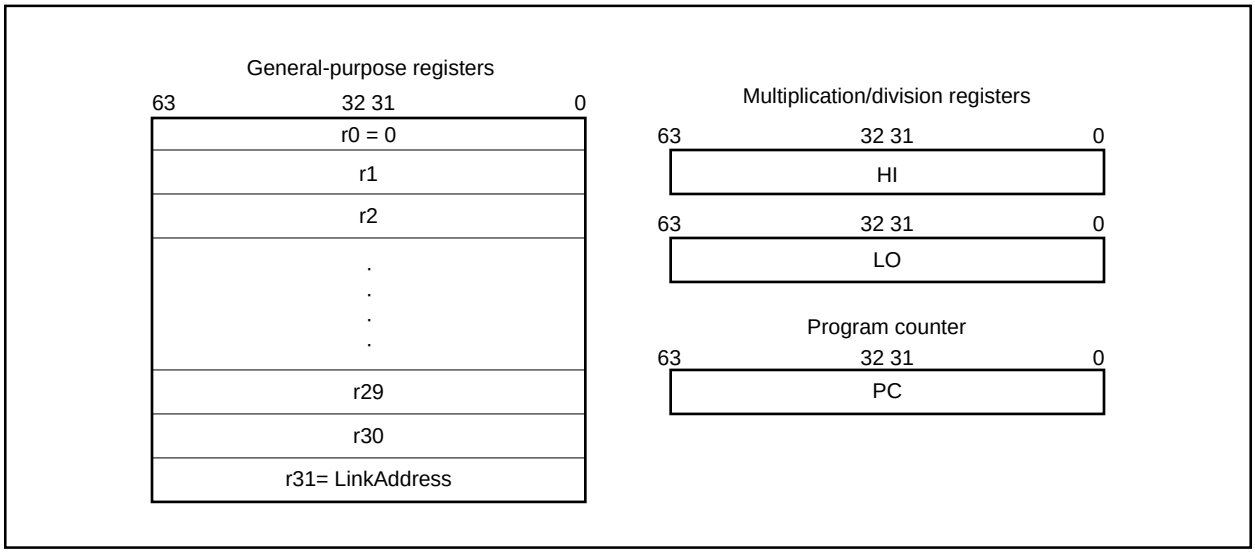
- Register r0 : The contents of this register are always 0. To discard the result of an operation, describe this register as the target of an instruction. When value 0 is necessary, this register can also be used as a source register.
- Register r31 : This is a link register used by link instructions, such as the Jump and Link (JAL) instruction. r31 can be used by other instructions. However, be careful that use of the register by a link instruction will not coincide with use of the register for other operations.

The two multiplication/division registers (HI and LO) store the result of multiplication or sum-of-products operation, or quotient (LO) and remainder (HI) resulting from division.

Because the VR4102 does not support floating-point instructions, it is not provided with the 32 floating-point general-purpose registers (FGR) found in the VR4300™ and VR4400™.

Remark The load link bit (LL bit) used with synchronization instructions (LL and SC) for multiprocessor supported by the VR4300 and VR4400 is not provided in the VR4102 (refer to **3.3 (2) Deletion of multiprocessor instructions**).

Figure 3-2. CPU Registers



The VR4102 does not have a program status word (PSW). The function of PSW is substituted by the status registers and cause registers incorporated to the system control coprocessor (CP0).

3.3 Outline of Instruction Set

Basically, the instruction set of the VR4102 conforms to the MIPS-I, -II, and -III instruction sets. However, it is different from those of the other processors in the VR series in the following four points. The difference between the VR4100 and VR4102 is that the VR4102 can manage operations including the peripheral functions by using power mode instructions (refer to **(4)**).

(1) Deletion of floating-point (FPU) instructions

Because the VR4102 does not have a floating-point unit, it does not support FPU instructions. If an FPU instruction is encountered, therefore, a reserved instruction exception occurs. If it is necessary to use an FPU instruction, emulate the instruction in software in an exception handler.

(2) Deletion of multiprocessor instructions

The VR4102 does not support a multiple processor operating environment. If a synchronization support instruction (LL or SC instruction) defined by MIPS-II and -III ISA is encountered, a reserved instruction exception occurs. In addition, the load link bit (LL bit) is also unavailable.

The VR4102 executes all load/store instructions in the programmed sequence. Therefore, the SYNC instruction is treated as a NOP instruction.

(3) Addition of sum-of-products instructions

The VR4102 has a dedicated sum-of-products operation core in the CPU and additional integer sum-of-products operation instructions, in order to execute sum-of-products operation at high speeds. Note that these instructions are not correctly executed with any other processors in the VR series.

The operations by the sum-of-products instructions are as follows:

(a) MADD16 (Multiply and Add 16-bit Integer)

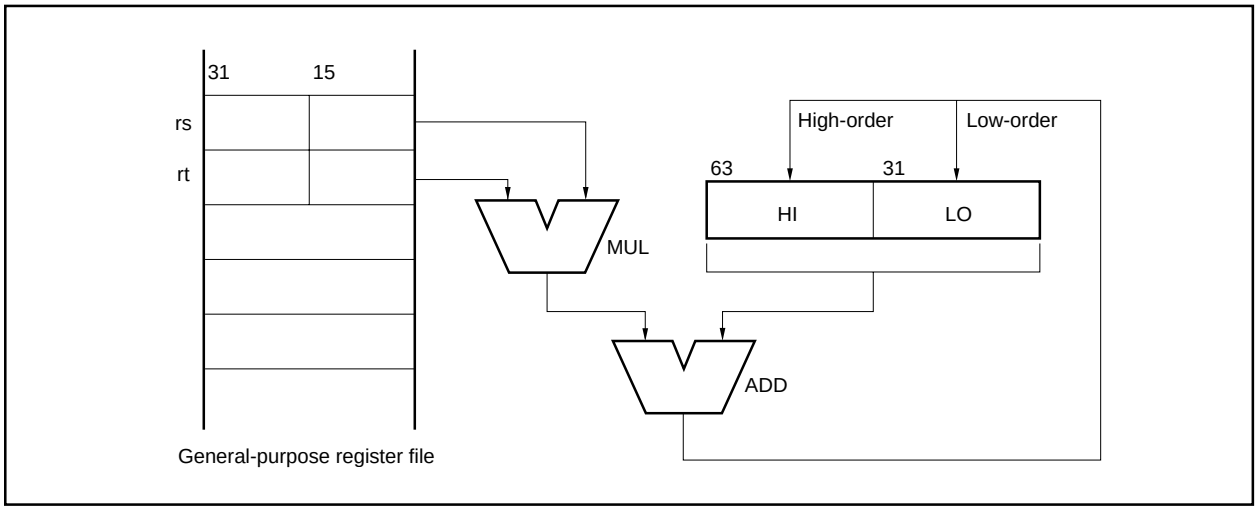
This instruction multiplies the contents of general-purpose register rs by the contents of general-purpose register rt. Both the operands are treated as signed 16-bit integers. Bits 62 through 15 of both the operands must be sign-extended.

The result of the multiplication is added to a 64-bit value combining special registers HI and LO. The low-order word (64 bits) of the result is loaded to special register LO, and the high-order word is loaded to HI.

An integer overflow exception does not occur.

Figure 3-3 outline the operation of the MADD16 instruction.

Figure 3-3. Operation of MADD16 Instruction



(b) DMADD16 (Doubleword Multiply and Add 16-bit register)

This instruction multiplies the contents of general-purpose register rs by the contents of general-purpose register rt. Both the operands are treated as signed 16-bit integers. Bits 62 through 15 of both the operands must be sign-extended.

The result of the multiplication is added to the value of special register LO. The result of the addition is treated as a signed integer. The 64-bit result is loaded to special register LO.

An integer overflow exception does not occur.

This operation is defined in the 64-bit mode and 32-bit kernel mode. If this instruction is encountered in the 32-bit user/supervisor mode, a reserved instruction exception occurs.

(4) Addition of power mode instructions

The VR4102 supports three power modes to lower the power consumption, and therefore, has dedicated instructions that set these modes. Note that the power mode instructions are not correctly executed by any other processors in the VR Series.

The operations of the power mode instructions are as follows:

(a) STANDBY

This instruction places the processor in the Standby mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus (internal) has entered the idle status, the internal clock is fixed to the high level, and the pipeline operation is stopped.

In the Standby mode, the PLL, clocks related to timers/interrupts, and interface clocks to the peripheral function blocks (TClock and MasterOut) operate normally.

When the processor is in the Standby mode it is returned to the Fullspeed mode by any interrupt including an internally generated timer interrupt.

(b) SUSPEND

This instruction places the processor in the Suspend mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus has entered the idle status, the internal clock and TClock are fixed to the high level, and the pipeline operation and interfacing to the peripheral function blocks are stopped.

In the Suspend mode, the PLL, clocks related to timers/interrupts, and MasterOut operate normally.

The processor remains in the Suspend mode until it accepts an interrupt. When the processor accepts an interrupt, it returns to the Fullspeed mode.

(c) HIBERNATE

This instruction places the processor in the Hibernate mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus has entered the idle status, all the clocks are fixed to the high level, and the pipeline operation is stopped.

The processor remains in the Hibernate mode until either the POWER pin is asserted active or the WakeUp timer interrupt occurs. The processor returns to the Fullspeed mode when the POWER pin is asserted active, when the WakeUp Timer interrupt occurs, or when the DCD# pin is asserted active.

The CPU and peripheral units, including clock-related units, stop their operations during the Hibernate mode.

3.4 System Control Coprocessor (CP0)

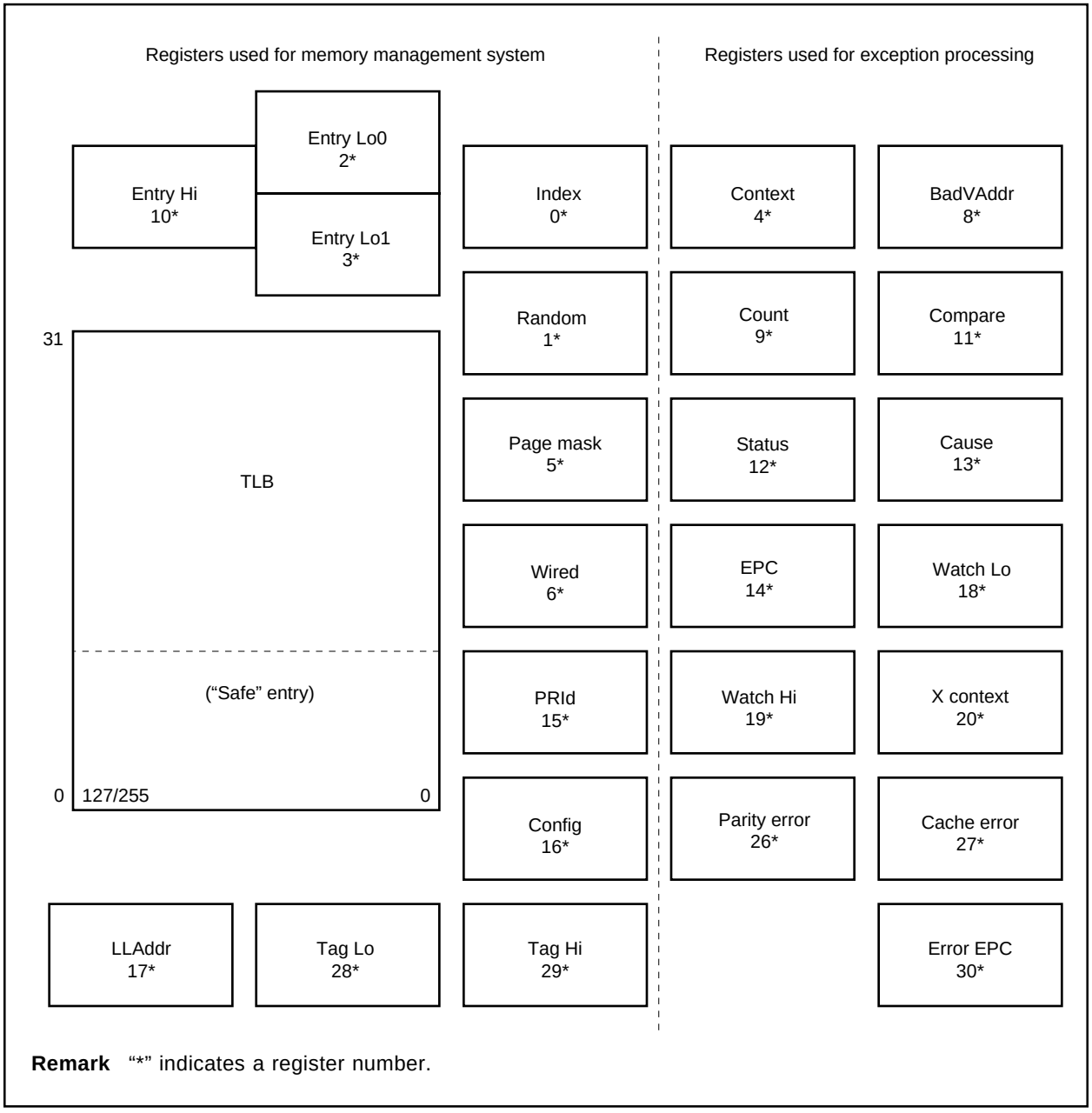
CP0 supports memory management, address translation, exception processing, and privilege operations. CP0 has the registers shown in Table 3-1, and a 32-entry TLB.

The basic configuration of the CP0 registers of the VR4102 is the same as that of the VR4300 and VR4400. However, because the number of entries of TLB, page size, cache size, physical address space, and system interface differ between the VR4102 and VR4300/VR4400, the bit configuration and setting differ. For details, refer to **VR4102 User's Manual**.

3.4.1 CP0 registers

All the CP0 registers that can be used with the VR4102 are listed below. Writing to or reading from an unused register (RFU) is undefined. In the 32-bit mode, the high-order 32 bits of 64-bit registers are masked.

Figure 3-4. CP0 Registers and TLB



Remark "*" indicates a register number.

Table 3-1. CP0 Registers

No.	Register	Description
0	Index	Programmable pointer to TLB array
1	Random	Dummy random pointer to TLB array (read-only)
2	Entry Lo0	Latter half of TLB entry for even-number VPN
3	Entry Lo1	Latter half of TLB entry for odd-number VPN
4	Context	Pointer to virtual PTE table of kernel in 32-bit mode
5	Page mask	Specifies page size
6	Wired	Number of wired TLB entries
7	—	RFU (Reserved for Future Use)
8	BadVAddr	Indicates virtual address at which error occurs last
9	Count	Timer count
10	Entry Hi	First half of TLB entry (including ASID)
11	Compare	Timer compare value
12	Status	Sets operation status
13	Cause	Indicates cause of last exception
14	EPC	Exception program counter
15	PRId	Processor revision ID
16	Config	Sets memory system mode
17	LLAddr	RFU
18	Watch Lo	Low-order bits of memory reference trap address
19	Watch Hi	High-order bits of memory reference trap address
20	X context	Pointer to virtual PTE table of kernel in 64-bit mode
21-25	—	RFU
26	Parity error	Parity bit of cache
27	Cache error	Error and status register of cache
28	Tag Lo	Cache tag register, low
29	Tag Hi	Cache tag register, high (reserved register)
30	Error EPC	Error exception program counter
31	—	RFU

3.5 Data Format and Addressing

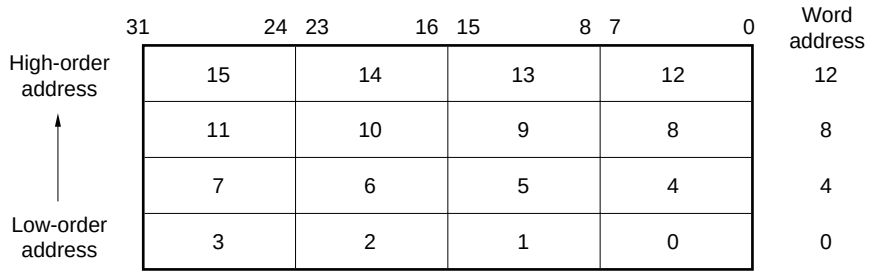
The VR4102 uses the following four data formats:

- Double word (64 bits)
- Word (32 bits)
- Half word (16 bits)
- Byte (8 bits)

The byte ordering is set by the BE bit of the config register. With the current VR4102, set little endian.

The byte ordering (endian) can be inverted during operation by setting the RE bit of the status register. However, be sure not to set this to 1 with the current VR4102.

Figure 3-5. Byte Address in Word: Little Endian



Remarks 1. The least significant byte is the lowest address.

2. A word is addressed by the address of the least significant byte.

Figure 3-6. Byte Address in Double Word: Little Endian

	Word				Half word			Byte	
	63			32	31	16	15 8	7 0	Double word address
High-order address	23	22	21	20	19	18	17	16	16
	15	14	13	12	11	10	9	8	8
Low-order address	7	6	5	4	3	2	1	0	0

Remarks 1. The least significant byte is the lowest address.

2. A word is addressed by the address of the least significant byte.

3.6 Virtual Storage

The VR4102 has a virtual storage management mechanism using TLB.

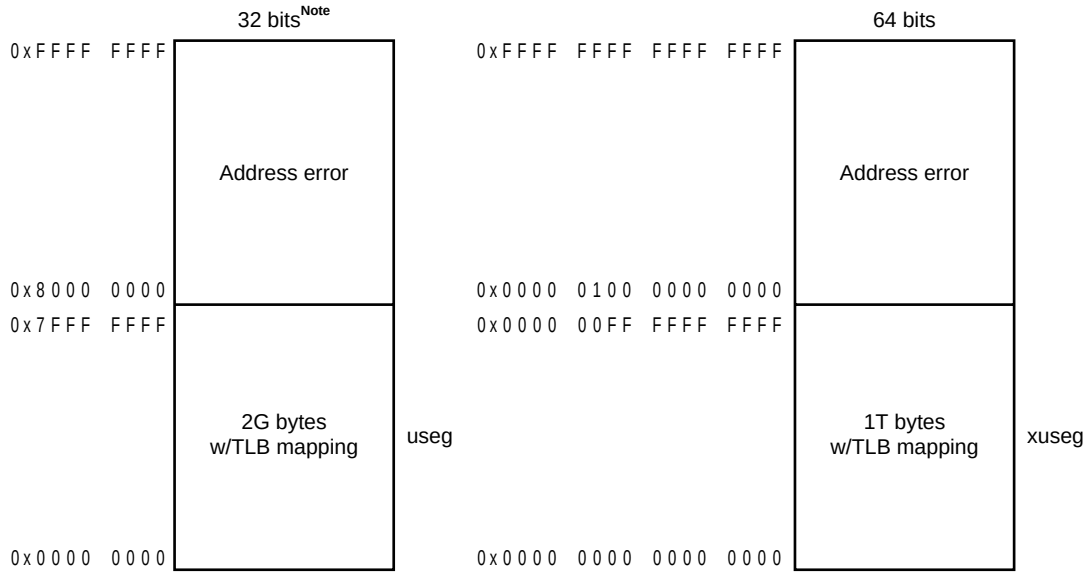
Virtual addresses are used for address management by software or address calculation of the pipeline. To access memories for program fetch and data access, and internal I/O and external I/O, physical addresses translated by TLB are used.

Note that part of the virtual address space is not translated by TLB, but is translated to physical addresses by merely changing specific addresses. If only this part of the address space is used, the VR4102 can be treated in the same manner as a CPU that operates with physical addresses.

3.6.1 Virtual address space

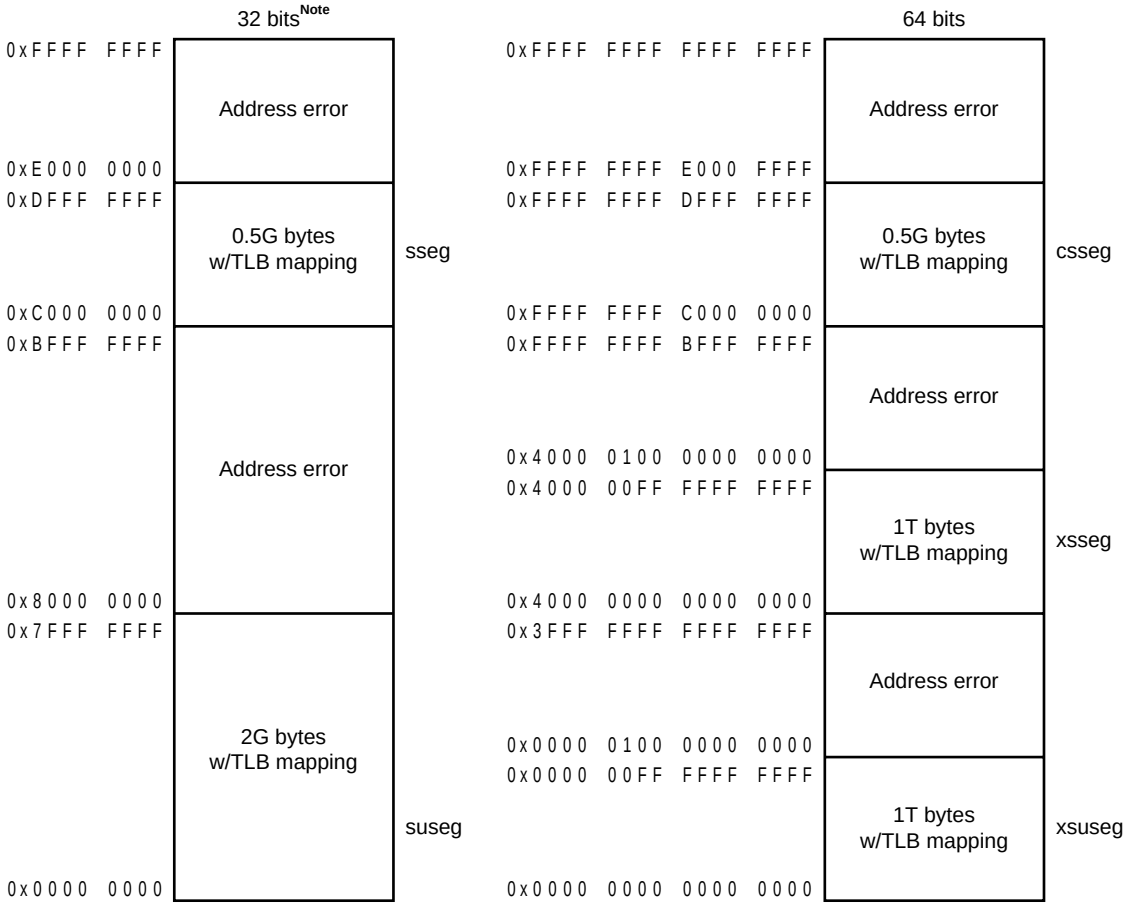
The VR4102 has two operation modes, 32-bit mode and 64-bit mode, and three types of operating modes: user mode, supervisor mode, and kernel mode. The virtual address space in each mode is shown below.

Figure 3-7. User Mode Address Space



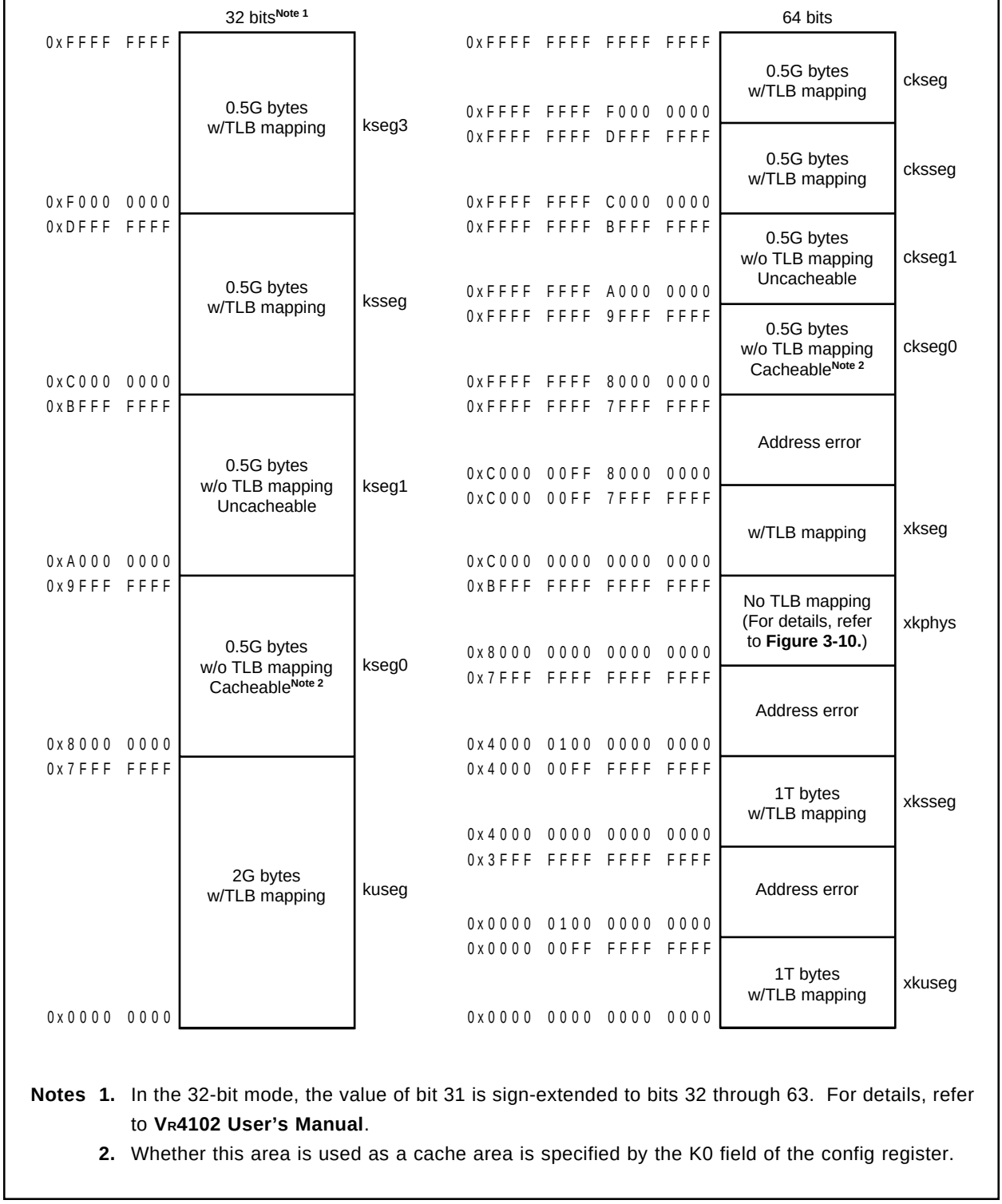
Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4102 User's Manual**.

Figure 3-8. Supervisor Mode Address Space



Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4102 User's Manual**.

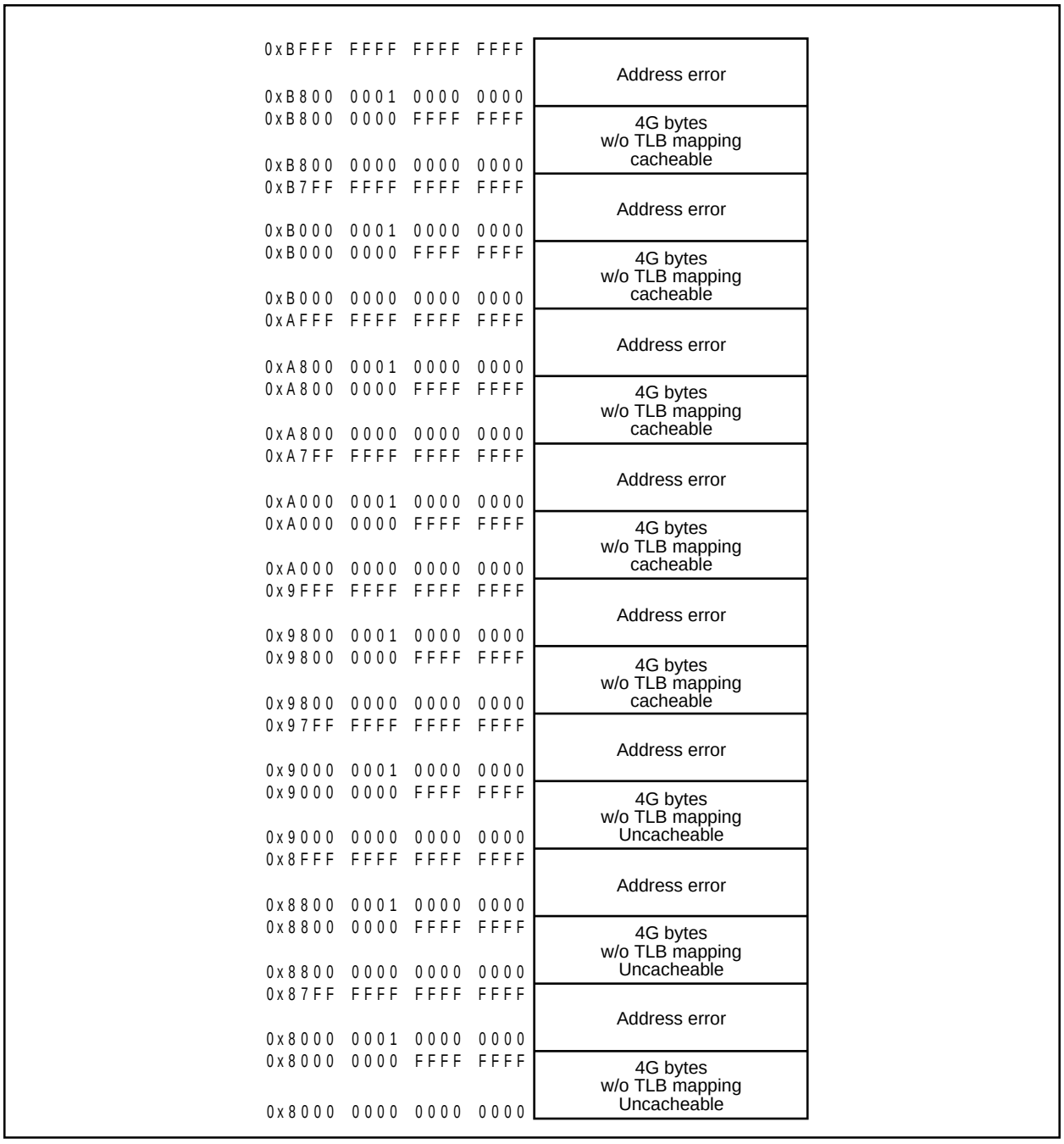
Figure 3-9. Kernel Mode Address Space



Notes 1. In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4102 User's Manual**.

2. Whether this area is used as a cache area is specified by the K0 field of the config register.

Figure 3-10. Details of xkphys Area



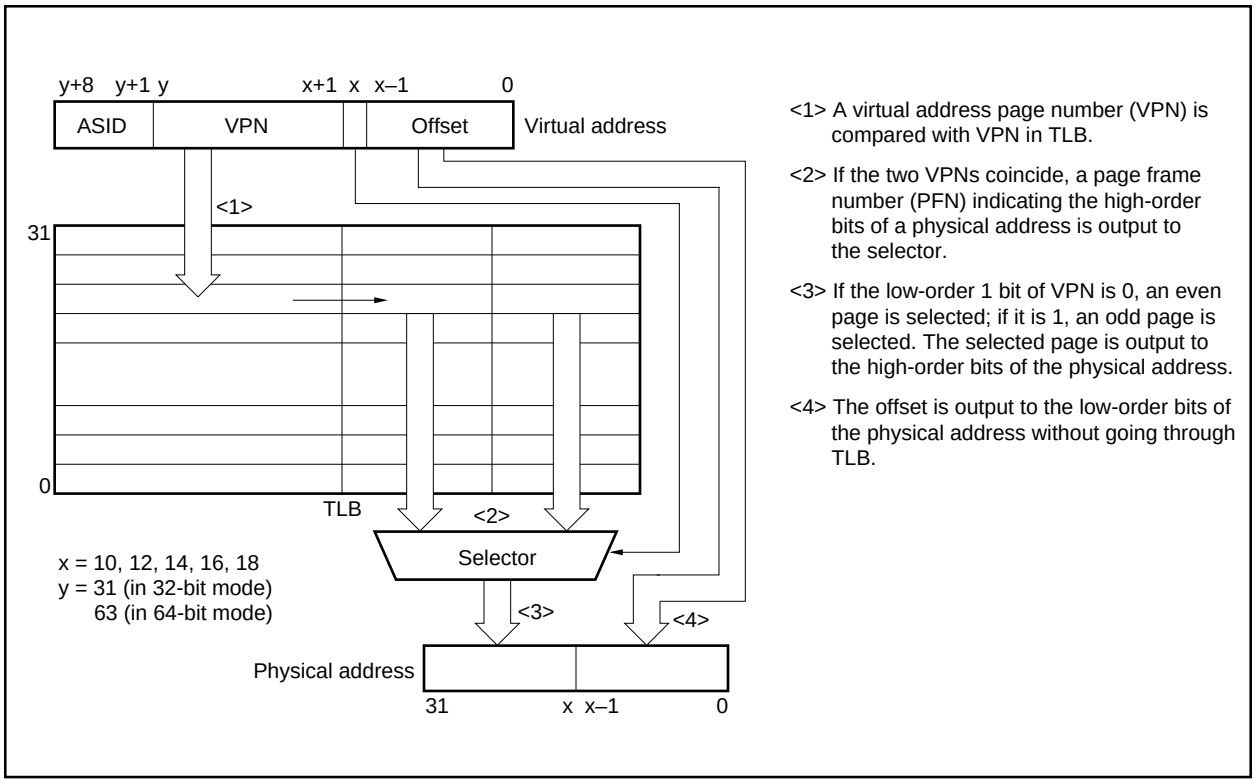
3.6.2 Address translation

Virtual addresses are translated into physical addresses by the internal TLB (Translation Lookaside Buffer) in page units. The TLB has a full-associative configuration and has 64 entries at the virtual address side and 32 entries at the physical address side. The page size is variable from 1 K to 256 Kbytes.

If a TLB entry is not found, a TLB non-coincidence exception occurs in the 32-bit mode, and an XTLB non-coincidence exception occurs in the 64-bit mode. Change the contents of the TLB in software.

The following figure outlines address translation.

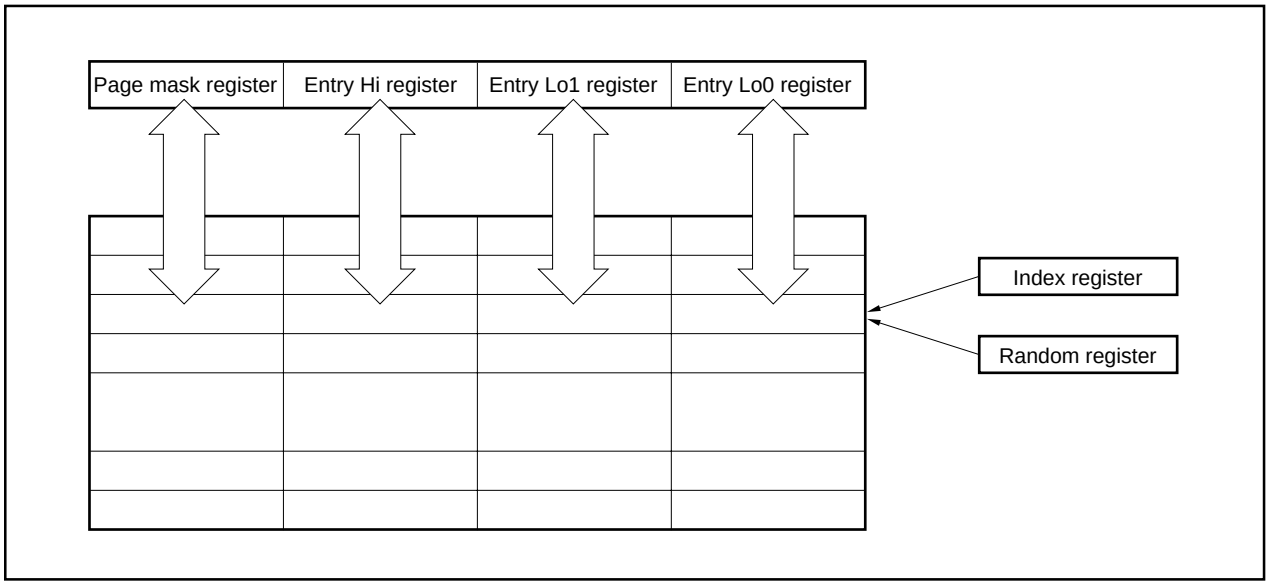
Figure 3-11. Outline of Address Translation



The TLB entry is read or written by loading/storing among the TLB entry indicated by the index register and random register, entry Hi, entry Lo1, entry Lo0, and page mask registers.

How the TLB is manipulated is illustrated below.

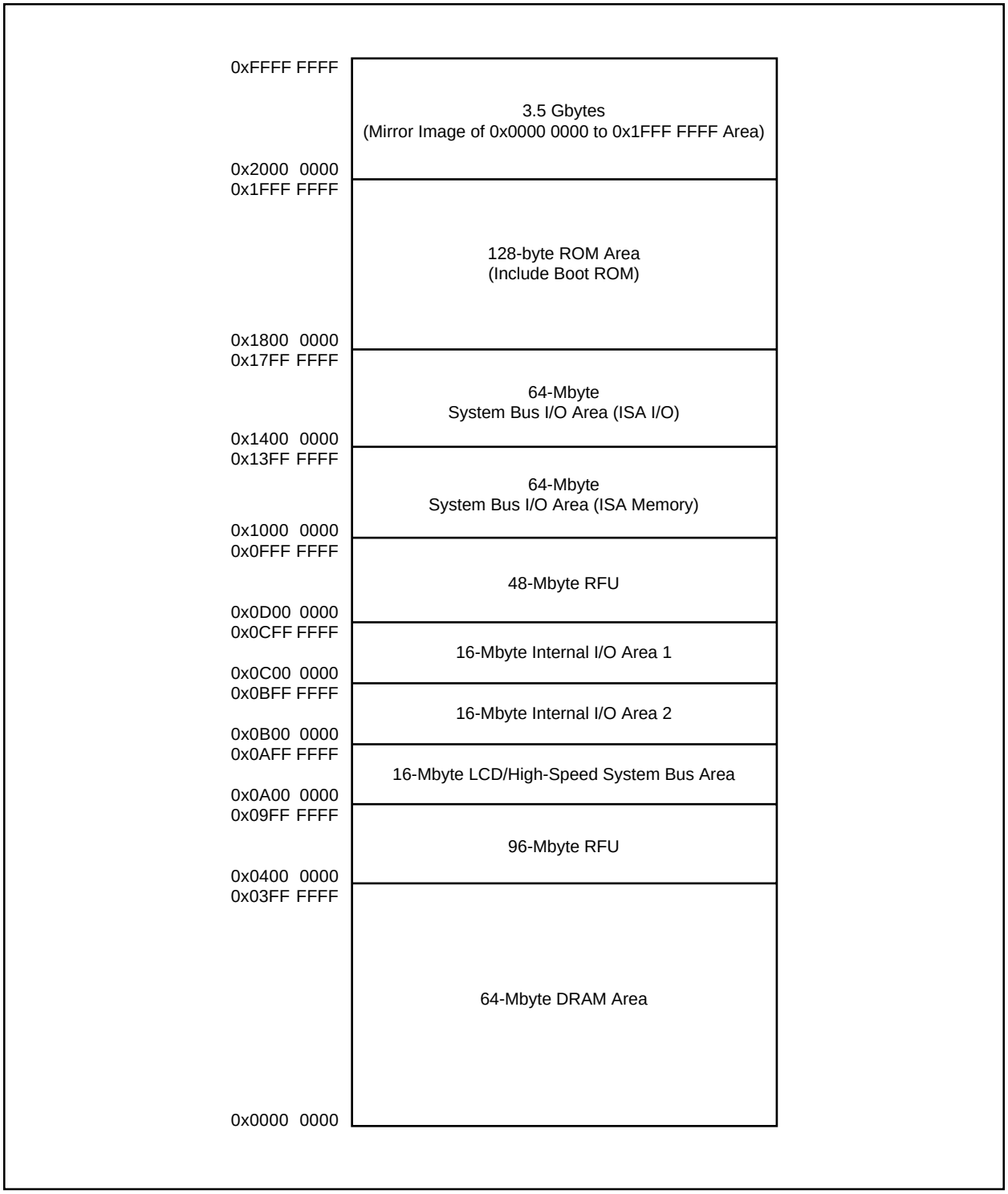
Figure 3-12. Outline of TLB Manipulation



3.7 Physical Address Space

Using a 32-bit address, the processor physical address space encompasses 4 Gbytes. The VR4102 uses this 4-Gbyte address space as shown in Figure 3-13.

Figure 3-13. VR4102 Physical Address Space



3.7.1 ROM address space

The ROM space differs depending on the bit width of the memory data bus and the capacity of the ROM being used.

- The bit width of the memory data bus is specified by the setting of the DBUS32 pin.
- The ROM capacity is set via the ROM64 bit of BCUCNTREG1.

The physical addresses of the ROM space are listed below.

Table 3-2. ROM Addresses (when using 16-bit data bus)

Physical address	ADD (25:0)	When using 32-Mbit ROM	When using 64-Mbit ROM
0x1FFF FFFF | 0x1FC0 0000	0x3FF FFFF | 0x0C0 0000	BANK 3 (ROMCS3#)	BANK 3 (ROMCS3#)
0x1FBF FFFF | 0x1F80 0000	0x3BF FFFF | 0x380 0000	BANK 2 (ROMCS2#)	
0x1F7F FFFF | 0x1F40 0000	0x37F FFFF | 0x340 0000	BANK 1 (ROMCS1#)	BANK 2 (ROMCS2#)
0x1F3F FFFF | 0x1F00 0000	0x33F FFFF | 0x300 0000	BANK 0 (ROMCS0#)	
0x1EFF FFFF | 0x1E80 0000	0x2FF FFFF | 0x280 0000	RFU	BANK 1 (ROMCS1#)
0x1E7F FFFF | 0x1E00 0000	0x27F FFFF | 0x200 0000		BANK 0 (ROMCS0#)
0x1DFF FFFF | 0x1800 0000	0x1FF FFFF | 0x000 0000		RFU

Table 3-3. ROM Addresses (when using 32-bit data bus)

Physical address	ADD (25:0)	When using 32-Mbit ROM	When using 64-Mbit ROM
0x1FFF FFFF | 0x1F80 0000	0x3FF FFFF | 0x380 0000	BANK 1 (ROMCS1#)	BANK 1 (ROMCS1#)
0x1F7F FFFF | 0x1F00 0000	0x37F FFFF | 0x300 0000	BANK 0 (ROMCS0#)	
0x1EFF FFFF | 0x1E00 0000	0x2FF FFFF | 0x200 0000	RFU	BANK 0 (ROMCS0#)
0x1DFF FFFF | 0x1800 0000	0x1FF FFFF | 0x000 0000		RFU

3.7.2 Internal I/O space

The VR4102 has two types of internal I/O spaces. Each of these spaces in the internal I/O space are described below.

Table 3-4. Internal I/O Space 1

Physical address	Internal I/O
0x0BFF FFFF – 0x0C00 0060	RFU
0x0C0 0005F – 0x0C00 0040	FIR
0x0C00 003F – 0x0C00 0020	HSP (software modem interface)
0x0C00 001F – 0x0C00 0000	SIU (16550)

Table 3-5. Internal I/O Space 2

Physical address	Internal I/O
0x0BFF FFFF – 0x0B00 02C0	RFU
0x0B00 02BF – 0x0B00 02A0	PIU2
0x0B00 029F – 0x0B00 0280	RFU
★ 0x0B00 027F – 0x0B00 0260	RFU
0x0B00 025F – 0x0B00 0240	LED
0x0B00 023F – 0x0B00 0220	RFU
0x0B00 021F – 0x0B00 0200	ICU2
0x0B00 01FF – 0x0B00 01E0	RUF
0x0B00 01DF – 0x0B00 01C0	RTC2
0x0B00 01BF – 0x0B00 01A0	DSIU
0x0B00 019F – 0x0B00 0180	KIU1
0x0B00 017F – 0x0B00 0160	AIU
0x0B00 015F – 0x0B00 0140	RFU
0x0B00 013F – 0x0B00 0120	PIU1
0x0B00 011F – 0x0B00 0100	GIU1
0x0B00 00FF – 0x0B00 00E0	DSU
0x0B00 00DF – 0x0B00 00C0	RTC1
0x0B00 00BF – 0x0B00 00A0	PMU
0x0B00 009F – 0x0B00 0080	ICU1
0x0B00 007F – 0x0B00 0060	CMU
0x0B00 005F – 0x0B00 0040	DCU
0x0B00 003F – 0x0B00 0020	DMAAU
0x0B00 001F – 0x0B00 0000	BCU

3.7.3 DRAM address space

The DRAM space differs depending on the bit width of the memory data bus and the capacity of the DRAM being used.

- The bit width of the memory data bus is specified by the setting of the DBUS32 pin.
- The DRAM capacity is set via the DRAM64 bit of BCUCNTREG1.

The physical addresses of the DRAM space are listed below.

Table 3-6. DRAM Addresses (when using 16-bit data bus)

Physical address	When using 16-Mbit DRAM	When using 64-Mbit DRAM
0x03FF FFFF – 0x0200 0000	RFU	RFU
0x01FF FFFF – 0x0180 0000		BANK 3 (MRAS3#/UUCAS#)
0x017F FFFF – 0x0100 0000		BANK 2 (MRAS2#/ULCAS#)
0x00FF FFFF – 0x0080 0000		BANK 1 (MRAS1#)
0x007F FFFF – 0x0060 0000	BANK 3 (MRAS3#/UUCAS#)	BANK 0 (MRAS0#)
0x005F FFFF – 0x0040 0000	BANK 2 (MRAS2#/ULCAS#)	
0x003F FFFF – 0x0020 0000	BANK 1 (MRAS1#)	
0x001F FFFF – 0x0000 0000	BANK 0 (MRAS0#)	

Table 3-7. DRAM Addresses (when using 32-bit data bus)

Physical address	When using 16-Mbit DRAM	When using 64-Mbit DRAM
0x03FF FFFF – 0x0200 0000	RFU	RFU
0x01FF FFFF – 0x0180 0000		BANK 1 (MRAS1#)
0x017F FFFF – 0x0100 0000		
0x00FF FFFF – 0x0080 0000		BANK 0 (MRAS0#)
0x007F FFFF – 0x0060 0000	BANK 1 (MRAS1#)	
0x005F FFFF – 0x0040 0000		
0x003F FFFF – 0x0020 0000	BANK 0 (MRAS0#)	
0x001F FFFF – 0x0000 0000		

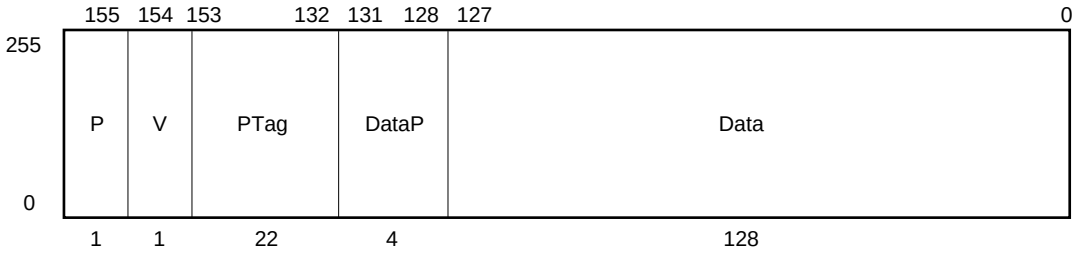
3.8 Cache

(1) Instruction cache

The instruction cache has the following features:

- Internal cache memory
- Capacity: 4 Kbytes
- Direct mapping mode
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-14. Format of Instruction Cache



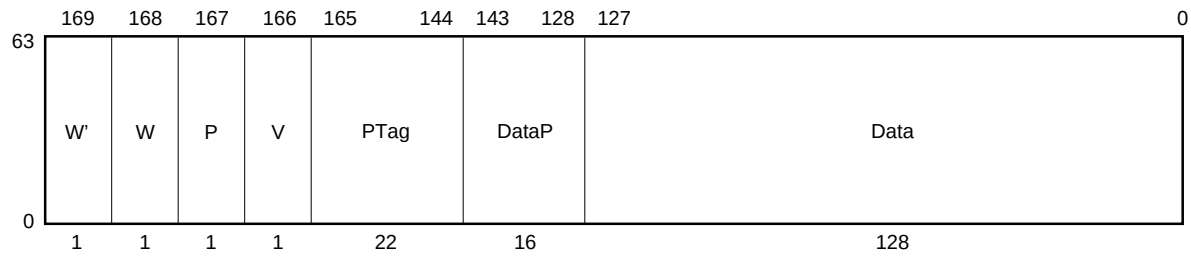
PTag : Physical tag (bits 31-10 of physical address)
V : Valid bit
Data : Cache data
P : Even parity for physical tag and V bit
DataP : Even parity for data (1-bit parity per 4-byte data)

(2) Data cache

The data cache has the following features:

- Internal cache memory
- Capacity: 1 Kbyte
- Write back
- Direct mapping mode
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-15. Format of Data Cache



W' : Even parity for write back bit
W : Write back bit
P : Even parity for physical tag and V bit
V : Valid bit
PTag : Physical tag (bits 31-10 of physical address)
DataP : Even parity for data (1-bit parity per 4-byte data)
Data : Cache data

3.9 Exception Processing

The VR4102 enters the kernel mode in which interrupts are disabled when an exception occurs, and executes an exception handler from a fixed exception vector address. To restore from the exception, the program counter, operating mode, and interrupt enable information must be restored to the original status. Save this information when the interrupt occurs.

When an interrupt occurs, the EPC register holds the address of the instruction that has caused the exception, or the address of the instruction immediately before if the exception has occurred in the branch delay slot. This means that the EPC register stores the address from which execution is to be started after the exception has been processed. At reset and on occurrence of NMI, the EPC register holds a restart address.

Table 3-8. Types of Exceptions

Exception	Symbol	Description
Cold reset	—	This exception occurs if the ColdReset# (internal) and Reset# (internal) signals are simultaneously asserted active (for details, refer to **Figures 4-1** through **4-5**). As a result, the instruction execution is stopped, and the handler on the reset vector is executed. The internal status, except some bits of the status registers, is undefined.
Soft reset	—	This exception occurs if the Reset# (internal) signal is asserted active. As a result, the instruction execution is stopped, and the handler on the reset vector is executed. The internal status before soft reset is retained. However, the current VR4102 does not support soft reset.
NIMI	—	This exception occurs if the NMI (internal) signal is asserted active.
TLB non-coincidence	TLBL/TLBS	This exception occurs if there is no TLB entry that coincides with an address to be referenced in the 32-bit mode.
Extended addressing TLB non-coincidence	TLBL/TLBS	This exception occurs if there is no TLB entry that coincides with an address to be referenced in the 64-bit mode.
TLB invalid	TLBL/TLBS	This exception occurs if the TLB entry that coincides with the virtual address to be referenced is invalid (V bit = 0).
TLB modify	Mod	This exception occurs if the TLB entry that coincides with the virtual address to be referenced is valid but is disabled from being written (D bit = 0) when the store instruction is executed.
Bus error	IBE/DBE	This exception occurs when the external agent indicates an error of data on the SysCmd bus by using an external interrupt to the bus interface (bus time-out, bus parity error, or invalid physical memory address or access type).
Address error	AdEL/AdES	This exception occurs if an attempt is made to execute the LH, SH/LW/SW, LD, or SD instruction to the half word/word/double word not located at the half word/word/double word boundary, or if an attempt is made to reference the virtual address that cannot be accessed.
Integer overflow	Ov	This exception occurs if a 2's complement overflow occurs as a result of addition or subtraction.
Trap	Tr	This exception occurs if the condition is true as a result of executing the trap instruction.
System call	Sys	This exception occurs if the SYSCALL instruction is executed.
Breakpoint	Bp	This exception occurs if the BREAK instruction is executed.
Reserved instruction	RI	This exception occurs if an instruction with an undefined op code (bits 31-26) or SPECIAL instruction with an undefined op code (bits 5-0) is executed.
Coprocessor non-usable	CpU	This exception occurs if the coprocessor instruction is executed when the corresponding coprocessor enable bit is not set.
Interrupt	Int	This exception occurs if one of the eight interrupt sources becomes active.
Cache error	—	This exception occurs if a parity error is detected in the internal cache or system interface.
Watch	WATCH	This exception occurs if an attempt is made to reference a physical address set by the watch Lo/Hi register with the load/store instruction.

The exception vectors and their offset values in the 64-bit and 32-bit modes are shown below.

Table 3-9. Base Address of Exception Vector in 64-Bit Mode (virtual address)

	Vector Base Address	Vector Offset
Cold reset, soft reset, NMI	0xFFFF FFFF BFC0 0000 (BEV bit is automatically set to 1.)	0x0000
Cache error	0xFFFF FFFF A000 0000 (BEV = 0) 0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0100
TLB non-coincidence, EXL =0	0xFFFF FFFF 8000 0000 (BEV = 0)	0x0000
XTLB non-coincidence, EXL = 0	0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0080
Others		0x0180

Table 3-10. Base Address of Exception Vector in 32-Bit Mode (virtual address)

	Vector Base Address	Vector Offset
Cold reset, soft reset, NMI	0xBFC0 0000 (BEV bit is automatically set to 1.)	0x0000
Cache error	0xA000 0000 (BEV = 0) 0xBFC0 0200 (BEV = 1)	0x0100
TLB non-coincidence, EXL =0	0x8000 0000 (BEV = 0)	0x0000
XTLB non-coincidence, EXL = 0	0xBFC0 0200 (BEV = 1)	0x0080
Others		0x0180

4. INITIALIZATION INTERFACE

This section explains the initialization interface and processor mode. Also explained are reset signal description and type, dependency of signals and timing, and initialization sequence in the mode the user can select.

Remark # in a signal name indicates active low.

4.1 Reset Function

The VR4102 can be reset in the following five ways. For details, refer to the **VR4102 User's Manual**.

4.1.1 RTC reset

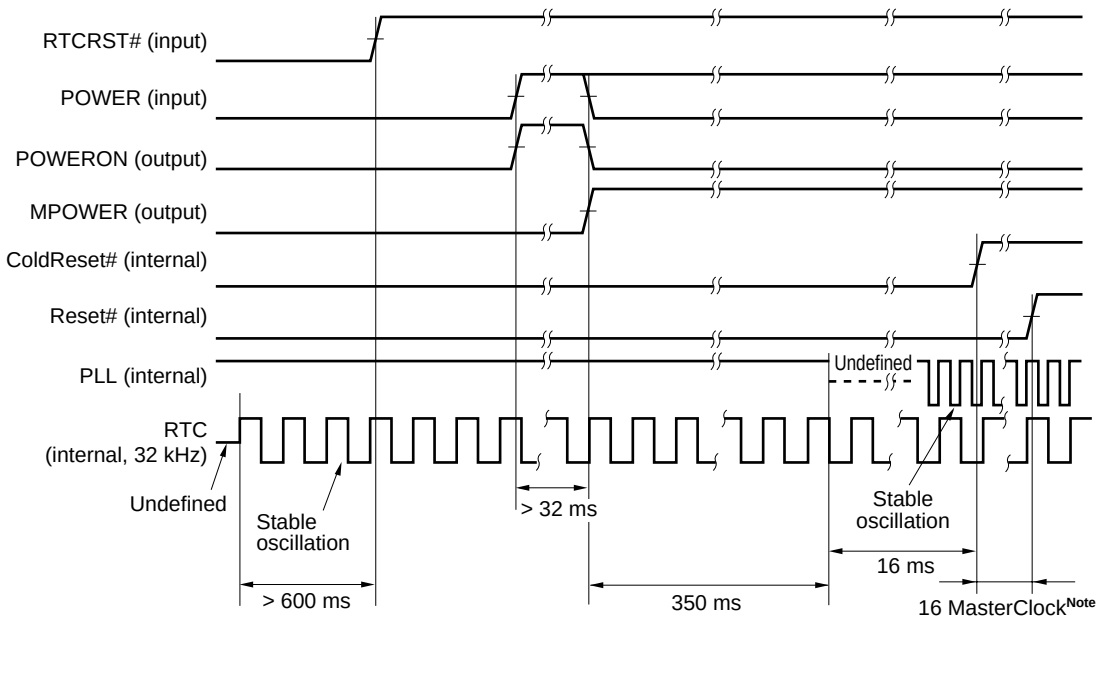
Assert the RTCRST# pin active on power application.

RTC reset does not save the status information at all, and completely initializes the internal status of the processor. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after RTC reset are not guaranteed.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4102 is reset, completely initialize the processor in software.

Figure 4-1. RTC Reset

★



Note MasterClock is the basic clock in the CPU core.

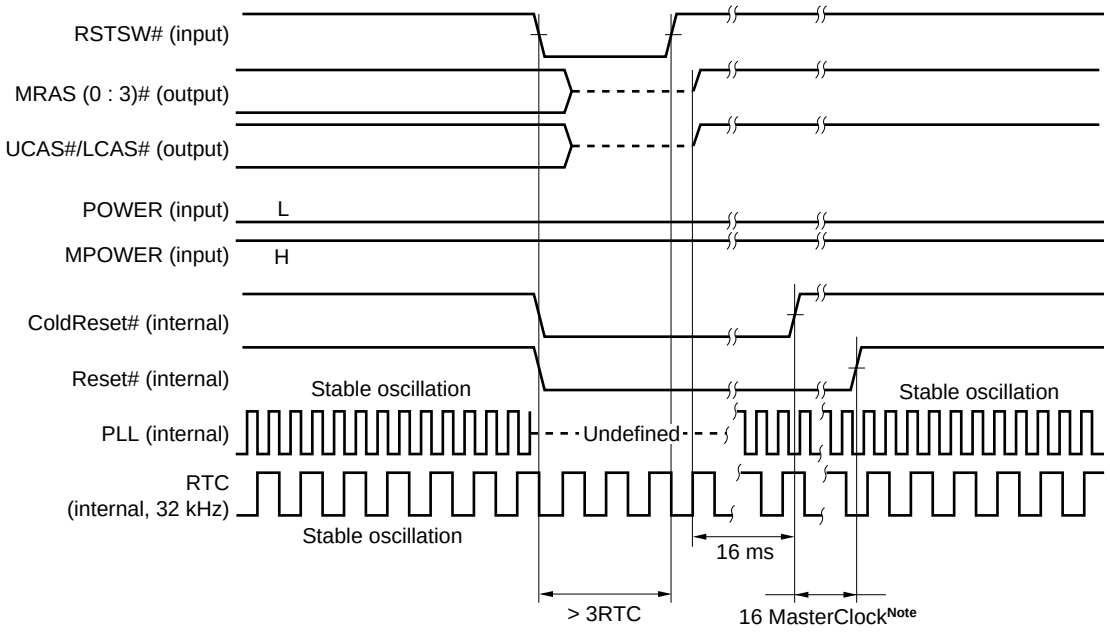
4.1.2 RSTSW

Assert the RSTSW# pin active.

Reset by RSTSW initializes all the internal statuses except the RTC timer and PMU. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after RSTSW reset are not guaranteed.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4102 is reset, completely initialize the processor in software.

Figure 4-2. RSTSW



Note MasterClock is the basic clock in the CPU core.

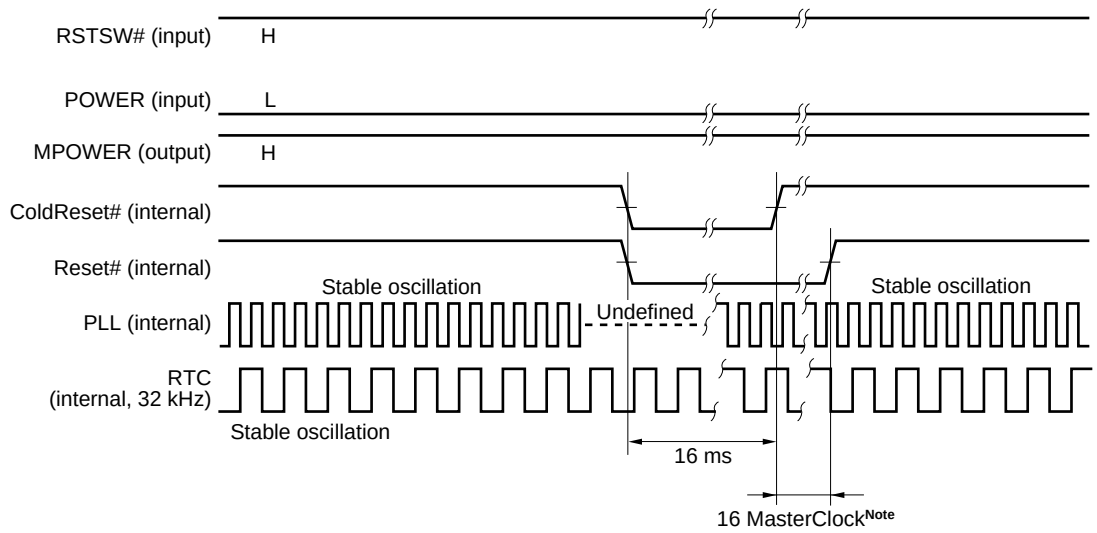
4.1.3 Deadman's SW

The VR4102 is reset if Deadman's SW is not cleared within a specific time after Deadman's SW was enabled.

Reset by Deadman's SW initializes all the internal statuses except the RTC timer and PMU. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after Deadman's SW reset are not guaranteed. For the setting of Deadman's SW, see **12. DSU (Deadman's SW Unit)**.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4102 is reset, completely initialize the processor in software.

Figure 4-3. Deadman's SW



Note MasterClock is the basic clock in the CPU core.

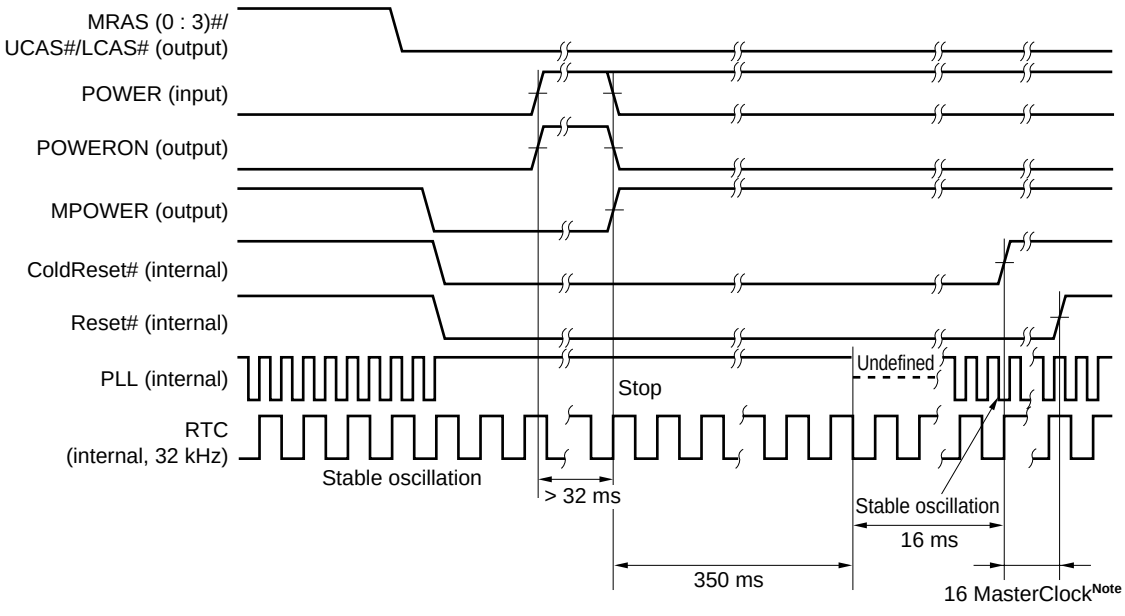
4.1.4 Software shutdown

When the software executes the HIBERNATE instruction, the VR4102 places the DRAM in the self-refresh mode, deasserts the MPOWER pin inactive, and enters the reset status.

Reset by software shutdown initializes all the internal statuses except the RTC timer and PMU.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4102 is reset, completely initialize the processor in software.

Figure 4-4. Software Shutdown



Note MasterClock is the basic clock in the CPU core.

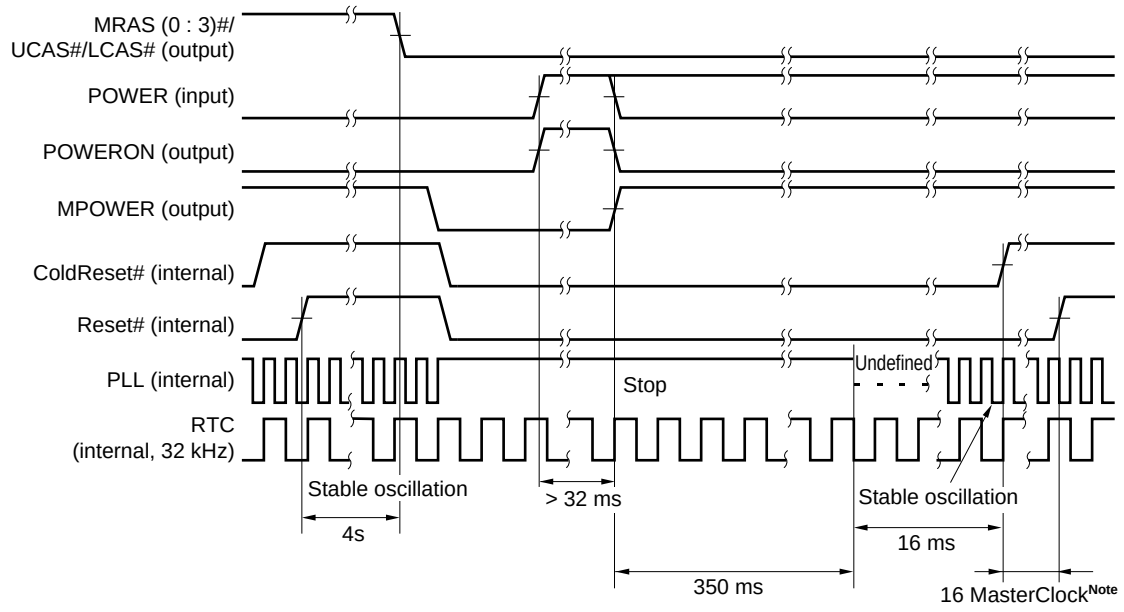
4.1.5 HALTimer shutdown

The VR4102 enters the reset status if HALTimer is not cleared by software within 4 seconds after RTC reset has been cleared.

Reset by HALTimer initializes all the internal statuses except the RTC timer and PMU.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4102 is reset, completely initialize the processor in software.

Figure 4-5. HALTimer Shutdown



Note MasterClock is the basic clock in the CPU core.

4.2 CPU Core Registers at Reset

Each of the CPU core registers is reset as follows:

- The TS and SR bits of the status register are cleared to 0.
- The ERL and BEV bits of the status register are set to 1.
- The upper-limit value (31) is set to the random register.
- The wired register is initialized to 0.
- Bits 31 through 28 of the config register are cleared to 0, and bits 22 through 3 are set to 0x04800. The other bits are undefined.
- The values of the registers other than above are undefined.

4.3 Power-On Sequence

The causes that change the status of the VR4102 from the Hibernate mode or shutdown status to the Fullspeed mode are called start causes. The start causes include asserting the POWERON pin active, asserting the DCD# pin active, alarm from the WakeUp timer, and asserting the GPIO (0:3), (9:12) pins active. When a start cause occurs, the VR4102 asserts the POWERON pin active to inform the external circuit that power to the VR4102 is about to be turned ON. Three RTC clocks after the POWERON pin has been asserted active, the VR4102 checks the status of the BATTINH pin. When the BATTINH pin is low, the VR4102 deasserts the POWERON pin inactive one RTC clock after checking the BATTINH or GPIO9 pin status, and is not started. If the BATTINH pin is high, the VR4102 deasserts the POWERON pin inactive three RTC clocks after the checking, asserts the MPOWER pin active, and is started.

Figure 4-6 shows the timing chart where the VR4102 is started. Figure 4-7 shows the timing chart where the VR4102 is not started because the BATTINH pin is low.

Figure 4-6. Start Sequence of VR4102 (if started)

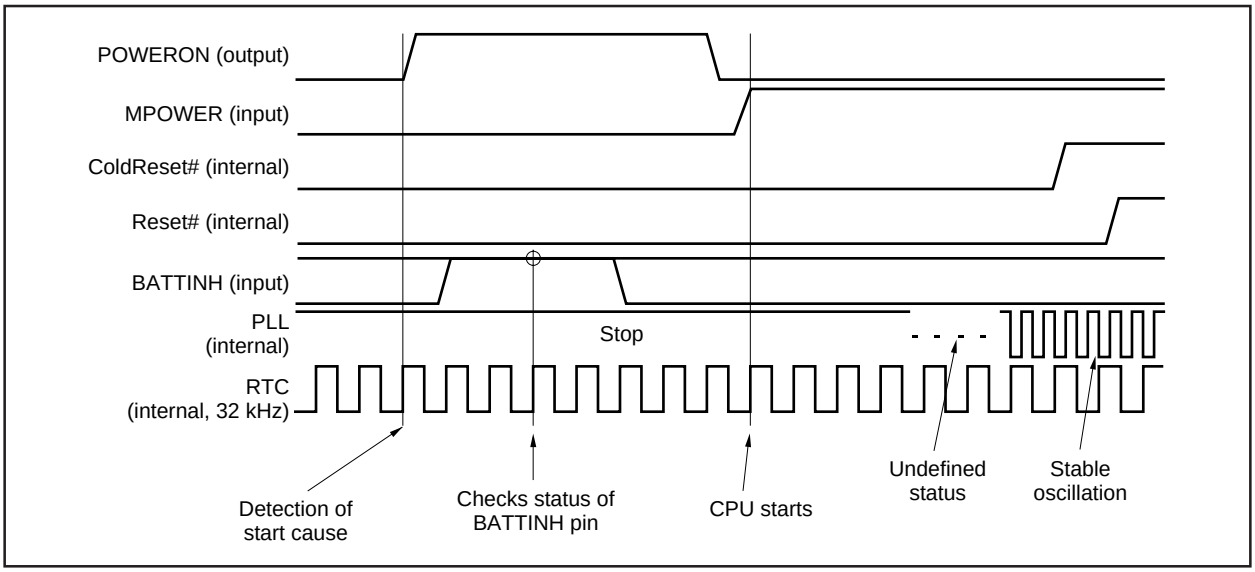
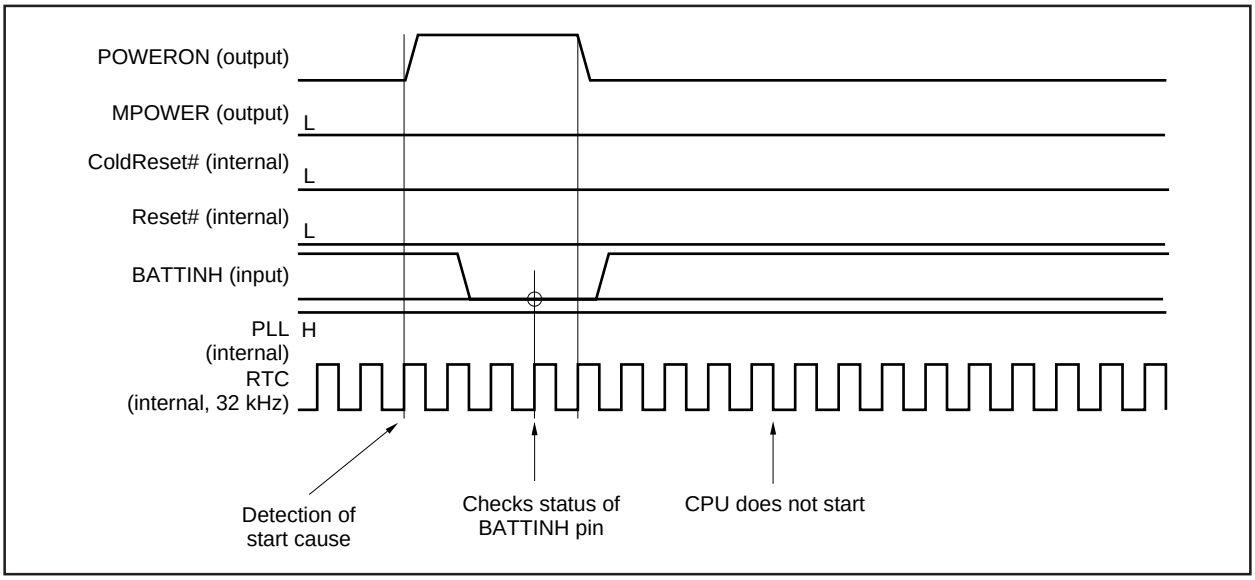


Figure 4-7. Start Sequence of VR4102 (if not started)



5. BCU (BUS CONTROL UNIT)

5.1 General

The BCU transfers data with the VR4100 CPU core via SysAD bus (internal) inside the VR4102. It also controls an external LCD controller, DRAM, ROM (flash memory or mask ROM), and PCMCIA controller via system bus, and transfers data with these devices via ADD bus and DATA bus.

For the timing chart between the VR4102 and each external device that is controlled by BCU, see **23. ELECTRICAL SPECIFICATIONS**.

Table 5-1. BCU Registers

Physical Address	Symbol	Function
0x0B00 0000	BCUCNTREG1	BCU control register 1
0x0B00 0002	BCUCNTREG2	BCU control register 2
0x0B00 000A	BCUSPEEDREG	BCU access cycle change register
0x0B00 000C	BCUERRSTREG	BCU bus error status register
0x0B00 000E	BCURFCNTREG	BCU refresh control register
0x0B00 0010	REVIDREG	Peripheral unit revision ID register
0x0B00 0012	BCURFCOUNTREG	BCU refresh cycle count register
0x0B00 0014	CLKSPEEDREG	Clock specify register

6. DMAAU (DMA ADDRESS UNIT)

6.1 General

DMAAU controls the addresses for the DMA operations between AIU/IrDA 4-Mbyte communication module (FIR) and memory.

The DMA start address of each DMA channel can be specified in a range of 0x0000 0000 through 0x01FF FFFE as a half-word address. The DMA space of each DMA channel is secured in a 2-Kbyte block that starts from the address generated by masking lower ten bits of the DMA start address to zero.

The DMA operation is not guaranteed if the DMA space overlaps with that of other peripheral units.

Table 6-1. DMAAU Registers

Physical Address	Symbol	Function
0x0B00 0020	AIUIBALREG	DMA base low-order address register for AIU input
0x0B00 0022	AIUIBAHREG	DMA base high-order address register for AIU input
0x0B00 0024	AIUIALREG	DMA low-order address register for AIU input
0x0B00 0026	AIUIAHREG	DMA high-order address register for AIU input
0x0B00 0028	AIUOBALREG	DMA base low-order address register for AIU output
0x0B00 002A	AIUOBAHREG	DMA base high-order address register for AIU output
0x0B00 002C	AIUOALREG	DMA low-order address register for AIU output
0x0B00 002E	AIUOAHREG	DMA high-order address register for AIU output
0x0B00 0030	FIRBALREG	DMA base low-order address register for FIR
0x0B00 0032	FIRBAHREG	DMA base high-order address register for FIR
0x0B00 0034	FIRALREG	DMA low-order address register for FIR
0x0B00 0036	FIRAHREG	DMA high-order address register for FIR

7. DCU (DMA CONTROL UNIT)

7.1 General

The DCU controls the DMA operation. It controls the DMA requests from the internal peripheral I/O units (FIR and AIU) and the acknowledge signal from the BCU that performs bus arbitration, and enables or disables the DMA operation.

Table 7-1. DCU Registers

Physical Address	Symbol	Function
0x0B00 0040	0020DMARSTREG	DMA reset register
0x0B00 0042	DMAIDLEREG	DMA sequencer status register
0x0B00 0044	DMASENREG	DMA sequencer enable register
0x0B00 0046	DMAMSKREG	DMA mask register
0x0B00 0048	DMAREQREG	DMA request register
0x0B00 004A	TDREG	Transfer direction set register

8. CMU (CLOCK MASK UNIT)

8.1 General

The CMU is used to specify whether the CPU core supplies the clock to each peripheral unit. By supplying the clock only to the necessary peripheral units, the power consumption can be reduced.

Table 8-1. CMU Register

Physical Address	Symbol	Function
0x0B00 0060	CMUCLKMSK	CMU clock mask register

9. ICU (INTERRUPT CONTROL UNIT)

9.1 General

The ICU receives an interrupt request signal from each peripheral unit and generates an interrupt request signal (Int0, Int1, Int2, Int3, or NMI) to the CPU core.

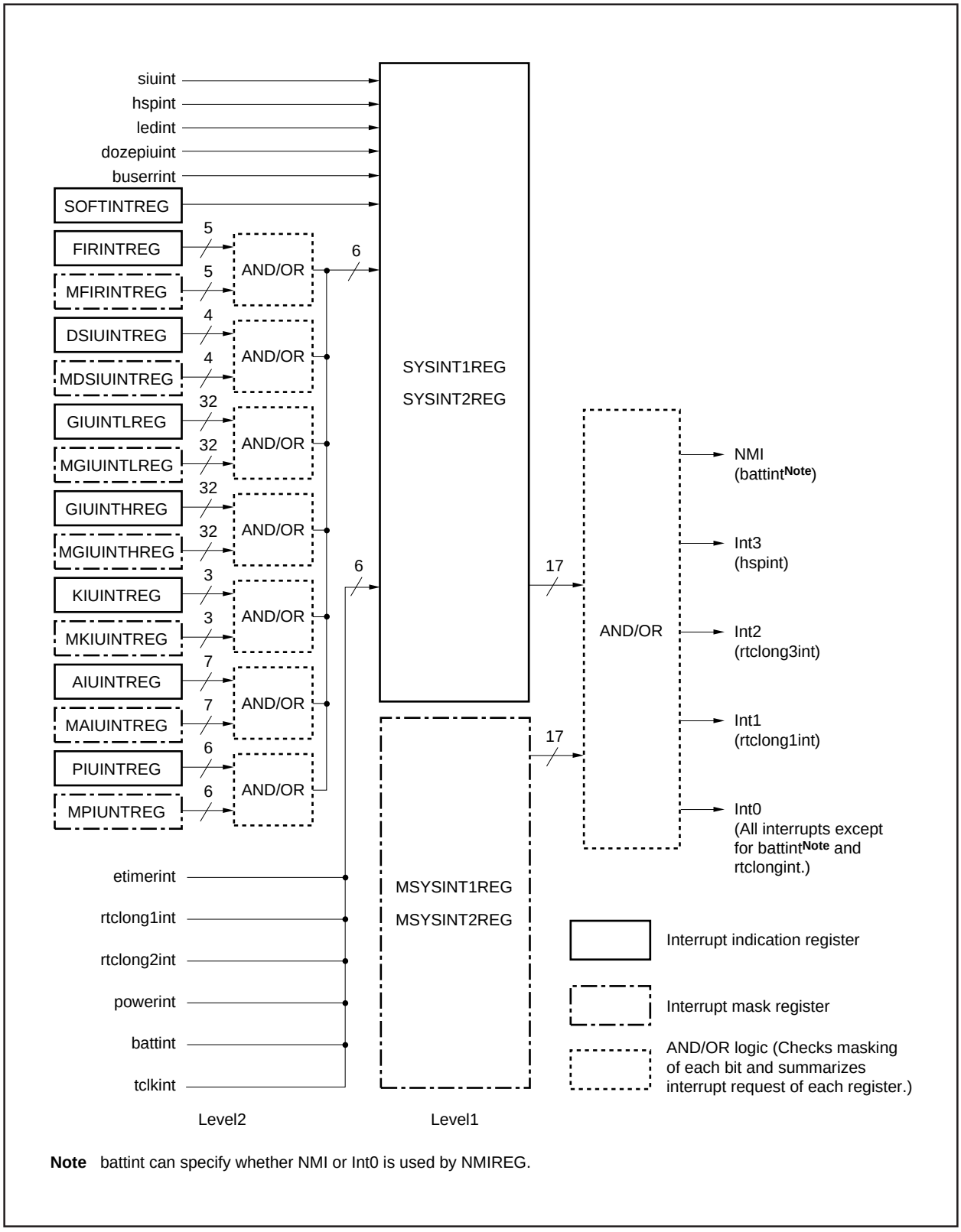
The function overview of ICU internal block is shown below.

Table 9-1. ICU Registers

Physical Address	Symbol	Function
0x0B00 0080	SYSINT1REG	System interrupt register1 (level 1)
0x0B00 0082	PIUINTREG	PIU interrupt register (level 2)
0x0B00 0084	AIUINTREG	AIU interrupt register(level 2)
0x0B00 0086	KIUINTREG	KIU interrupt register (level 2)
0x0B00 0088	GIUINTLREG	GIU interrupt low-order address register (level 2)
0x0B00 008A	DSIUINTREG	DSIU interrupt register (level 2)
0x0B00 008C	MSYSINT1REG	System interrupt mask register 1 (level 1)
0x0B00 008E	MPIUINTREG	PIU interrupt mask register (level 2)
0x0B00 0090	MAIUINTREG	AIU interrupt mask register (level 2)
0x0B00 0092	MKIUINTREG	KIU interrupt mask register (level 2)
0x0B00 0094	MGIUINTLREG	GIU interrupt mask low-order address register (level 2)
0x0B00 0096	MDSIUINTREG	DSIU interrupt mask register (level 2)
0x0B00 0098	NMIREG	Battery interrupt select register
0x0B00 009A	SOFTINTREG	Software interrupt register
0x0B00 0200	SYSINT2REG	System interrupt register 2 (level 1)
0x0B00 0202	GIUINTHREG	GIU interrupt high-order address register (level 2)
0x0B00 0204	FIRINTREG	FIR interrupt register (level 2)
0x0B00 0206	MSYSINT2REG	System interrupt mask register 2 (level 1)
0x0B00 0208	MGIUINTHREG	GIU interrupt mask high-order address register (level 2)
0x0B00 020A	MFIRINTREG	FIR interrupt mask register (level 2)

9.2 Configuration

Figure 9-1. ICU Configuration



Note battint can specify whether NMI or Int0 is used by NMIREG.

10. PMU (POWER MANAGEMENT UNIT)

10.1 General

PMU manages and controls power to the internal and external circuits of the VR4102 as follows:

- Controls shutdown
- Controls reset
- Controls power-ON
- Controls low-power consumption mode

PMU also set the start cause via the GPIO (0:3), (9:12) pins and DCD# pin.

Table 10-1. PMU Registers

Physical Address	Symbol	Function
0x0B00 00A0	PMUINTREG	PMU interrupt/status register
0x0B00 00A2	PMUCNTREG	PMU control register

10.2 Power Mode

The VR4102 supports the following four power modes:

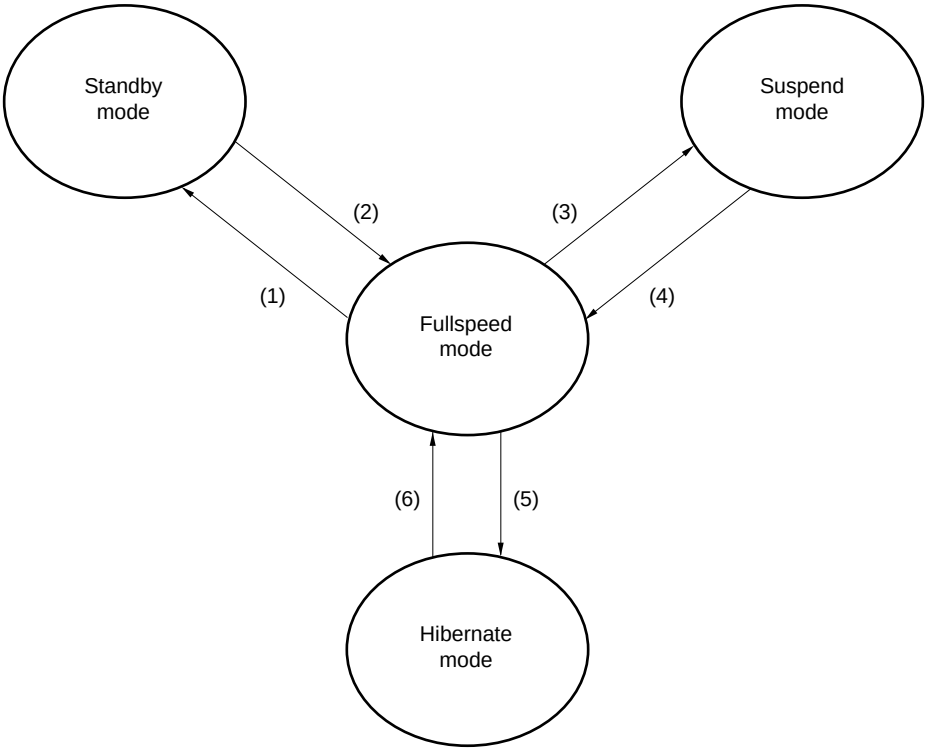
- Fullspeed mode
- Standby mode
- Suspend mode
- Hibernate mode

Figure 10-1 illustrates the transition of the power modes.

To change the mode from Fullspeed to Standby, Suspend, or Hibernate, execute the STANDBY, SUSPEND, or HIBERNATE instruction. To change the mode from Standby, Suspend, or Hibernate to Fullspeed, either generate an interrupt, or execute a reset operation.

Table 10-2 outlines each power mode.

Figure 10-1. Power Mode Transition



(1)	(2)	(3)	(4)	(5)	(6)
STANDBY instruction, pipeline flash, SysAD idle, PClock high level	All interrupts	SUSPEND instruction, pipeline flash, SysAD idle, PClock high level, TClock high level, DRAM self refresh start	BatteryInt POWERSW RTCRST Alarm KeyTouch PenTouch GPIO (0:3) pins GPIO (9:12) pins DCD# pin	HIBERNATE instruction, pipeline flash, SysAD idle, PClock high level, TClock high level, MasterOut high level, DRAM self refresh start	POWERSW Alarm DCD# pin GPIO (0:3) pins GPIO (9:12) pins

Table 10-2. Outline of Power Mode

Mode	Internal Peripheral Unit				Pipe line
	RTC	ICU	DCU	Others	
Fullspeed	On	On	On	Selectable[Note]	On
Standby	On	On	On	Selectable[Note]	Off
Suspend	On	On	Off	Off	Off
Hibernate	On	Off	Off	Off	Off
Off	Off	Off	Off	Off	Off

Note Refer to **8. CMU (CLOCK MASK UNIT)**.

11. RTC (REAL-TIME CLOCK UNIT)

11.1 General

The RTC consists of the following three types of timers.

- RTCLong timer (two timers)
  This is a 24-bit programmable down counter that counts down at a cycle of 32.768 kHz. It can generate an interrupt request at intervals of up to 512 seconds.
- ElapsedTime timer (one timer)
  This is a 48-bit up counter that counts up at a cycle of 32.768 kHz. When this counter counts up to about 272 years, it returns to 0. This counter consists of an 48-bit comparator (ECMPHREG, ECMPLREG, ECMPMREG) and a 48-bit alarm time register (ETIMELREG, ETIMEMREG, ETIMEHREG). By comparing these, an interrupt request can be generated at specific time.
- TClock count timer (one timer)
  This is a 25-bit programmable counter that counts down at each TClock cycle. Interrupt requests can be generated with a cycle of up to 2 seconds by setting the CLKSEL pin. This timer is used for performance evaluation.

Table 11-1. RTC Registers

Physical Address	Symbol	Function
0x0B00 00C0	ETIMELREG	Elapsed Time timer register, low
0x0B00 00C2	ETIMEMREG	Elapsed Time timer register, middle
0x0B00 00C4	ETIMEHREG	Elapsed Time timer register, high
0x0B00 00C8	ECMPLREG	Elapsed Time timer compare register, low
0x0B00 00CA	ECMPMREG	Elapsed Time timer compare register, middle
0x0B00 00CC	ECMPHREG	Elapsed Time timer compare register, high
0x0B00 00D0	RTCL1LREG	RTCLong 1 timer register, low
0x0B00 00D2	RTCL1HREG	RTCLong 1 timer register, high
0x0B00 00D4	RTCL1CNTLREG	RTCLong 1 timer count register, low
0x0B00 00D6	RTCL1CNTHREG	RTCLong 1 timer count register, high
0x0B00 00D8	RTCL2LREG	RTCLong 2 timer register, low
0x0B00 00DA	RTCL2HREG	RTCLong 2 timer register, high
0x0B00 00DC	RTCL2CNTLREG	RTCLong 2 timer count register, low
0x0B00 00DE	RTCL2CNTHREG	RTCLong 2 timer count register, high
0x0B00 01C0	TCLKLREG	TClock counter register, low
0x0B00 01C2	TCLKHREG	TClock counter register, high
0x0B00 01C4	TCLKCNTLREG	TClock counter count register, low
0x0B00 01C6	TCLKCNTHREG	TClock counter count register, high
0x0B00 01CE	RTCINTREG	RTC interrupt register

12. DSU (Deadman's SW Unit)

12.1 General

The DSU automatically detects a hang-up of the VR4102 and resets the VR4102. By stopping a hang-up at the earliest stage by using the DSU, the destruction of data can be minimized.

The DSU can set for a cycle of up to 15 seconds in units of 1 second. Set the DSWCLR bit of the DSUCLRREG register to 1 within this time in software. If the bit is not set within the time, the CPU is reset (refer to **4. INITIALIZATION INTERFACE**).

Table 12-1. DSU Registers

Physical Address	Symbol	Function
0x0B00 00E0	DSUCNTREG	DSU control register
0x0B00 00E2	DSUSETREG	DSU cycle set register
0x0B00 00E4	DSUCLRREG	DSU clear register
0x0B00 00E6	DSUTIMREG	DSU elapsed time register

13. GIU (GENERAL-PURPOSE I/O UNIT)

13.1 General

GIU controls GPIO and DCD# pins. The GPIO pins constitute a general-purpose I/O port. GIU can assign the interrupt request signal function for these pins. As a trigger, the edge of the input signal (rising or falling edge), high level, or low level can be selected. Use the PMUCNTREG register of PMU, however, to specify the start cause via the GPIO (0:3), GPIO (9:12), or DCD# pin.

Table 13-1. GIU Registers

Physical Address	Symbol	Function
0x0B00 0100	GIUIOSELL	GPIO input/output setting register L
0x0B00 0102	GIUIOSELH	GPIO input/output setting register H
0x0B00 0104	GIUPIODL	GPIO input/output data register L
0x0B00 0106	GIUPIODH	GPIO input/output data register H
0x0B00 0108	GIUINTSTATL	GPIO interrupt register L
0x0B00 010A	GIUINTSTATH	GPIO interrupt register H
0x0B00 010C	GIUINTENL	GPIO interrupt enable register L
0x0B00 010E	GIUINTENH	GPIO interrupt enable register H
0x0B00 0110	GIUINTTYPL	GPIO interrupt trigger setting register L
0x0B00 0112	GIUINTTYPH	GPIO interrupt trigger setting register H
0x0B00 0114	GIUINTALSELL	GPIO interrupt level setting register L
0x0B00 0116	GIUINTALSELH	GPIO interrupt level setting register H
0x0B00 0118	GIUINTHTSELL	GPIO interrupt hold setting register L
0x0B00 011A	GIUINTHTSELH	GPIO interrupt hold setting register H
0x0B00 011C	GIUPODATL	GPIO output data register L
0x0B00 011E	GIUPODATH	GPIO output data register H

Table 13-2. Outline of GPIO pins

Pin	Interrupt Request Detection Clock (internal)	Input Buffer Type	Output Clock
GPIO (49:32)	—	—	TClock
GPIO (31:16)	TClock	Normal	TClock
GPIO15 (DCD#)	MasterOut	Normal	—
GPIO (14:9)	MasterOut	Normal	MasterOut
★ GPIO (8:5)	TClock	Normal	TClock
★ GPIO4	TClock	Schmitt	TClock
★ GPIO (3:0)	RTC	Schmitt	RTC

Caution Pin GPIO15 cannot be used as a general-purpose I/O pin because its function is fixed to DCD# signal input.

14. PIU (TOUCH PANEL UNIT)

14.1 General

PIU uses an on-chip 10-bit A/D converter and detects the X and Y coordinates of pen contact locations on the touch panel, and scans the general-purpose A/D input port. Since the touch panel control circuit and the A/D converter (conversion precision: 10 bits) are both on-chip, the touch panel can be connected directly to the VR4102.

Figure 14-1. PIU Peripheral Block Diagram

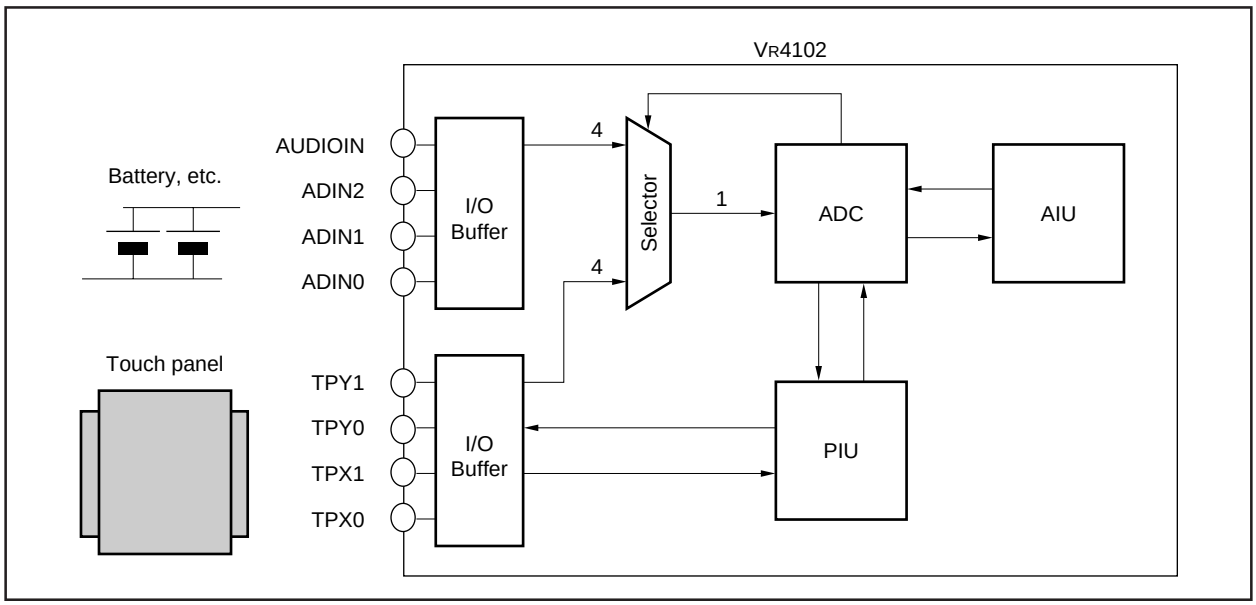


Table 14-1. PIU Registers

Physical Address	Symbol	Function
0x0B00 0122	PIUCNTREG	PIU control register
0x0B00 0124	PIUINTREG	PIU interrupt register
0x0B00 0126	PIUSIVLREG	PIU data sampling cycle set register
0x0B00 0128	PIUSTBLREG	PIU A/D converter wait time set register
0x0B00 012A	PIUCMDREG	PIU A/D command register
0x0B00 0130	PIUASCNREG	PIU A/D port scan register
0x0B00 0132	PIUAMSKREG	PIU A/D scan mask register
0x0B00 013E	PIUCIVLREG	PIU count register
0x0B00 02A0	PIUPB00REG	PIU page 0 buffer 0 register
0x0B00 02A2	PIUPB01REG	PIU page 0 buffer 1 register
0x0B00 02A4	PIUPB02REG	PIU page 0 buffer 2 register
0x0B00 02A6	PIUPB03REG	PIU page 0 buffer 3 register
0x0B00 02A8	PIUPB10REG	PIU page 1 buffer 0 register
0x0B00 02AA	PIUPB11REG	PIU page 1 buffer 1 register
0x0B00 02AC	PIUPB12REG	PIU page 1 buffer 2 register
0x0B00 02AE	PIUPB13REG	PIU page 1 buffer 3 register
0x0B00 02B0	PIUAB0REG	PIU A/D scan buffer 0 register
0x0B00 02B2	PIUAB1REG	PIU A/D scan buffer 1 register
0x0B00 02B4	PIUAB2REG	PIU A/D scan buffer 2 register
0x0B00 02B6	PIUAB3REG	PIU A/D scan buffer 3 register
0x0B00 02BC	PIUPB04REG	PIU page 0 buffer 4 register
0x0B00 02BE	PIUPB14REG	PIU page 1 buffer 4 register

15. SIU (SERIAL INTERFACE UNIT)

15.1 General

SIU is a serial interface that conforms to the RS-232C communication standard and is equipped with two one-channel interfaces, one for transmission and one for reception.

SIU is functionally compatible with the NS16550, and supports a transfer rate up to 1.152-Mbps. This unit also has an infrared communication function that corresponds to SIR.

Table 15-1. SIU Registers

Physical Address	LCR7	R/W	Symbol	Function
0x0C00 0000	0	R	SIURB	Receive buffer register (Read)
		W	SIUTH	Transmission hold register (Write)
	1	R/W	SIUDLL	Division ratio low-order byte register
0x0C00 0001	0	R/W	SIUIE	Interrupt enable register
	1	R/W	SIUDLM	Division ratio high-order byte register
0x0C00 0002	—	R	SIUIID	Interrupt identification register (Read)
		W	SIUFC	FIFO control register (Write)
0x0C00 0003	—	R/W	SIULC	Line control register
0x0C00 0004	—	R/W	SIUMC	Modem control register
0x0C00 0005	—	R/W	SIULS	Line status register
0x0C00 0006	—	R/W	SIUMS	Modem status register
0x0C00 0007	—	R/W	SIUSC	Scratch register
0x0C00 0008	—	R/W	SIUIRSEL	Serial communication select register

Remark LCR7 is bit 7 of the SIULC register.

15.2 Configuration

Figure 15-1. SIU Configuration

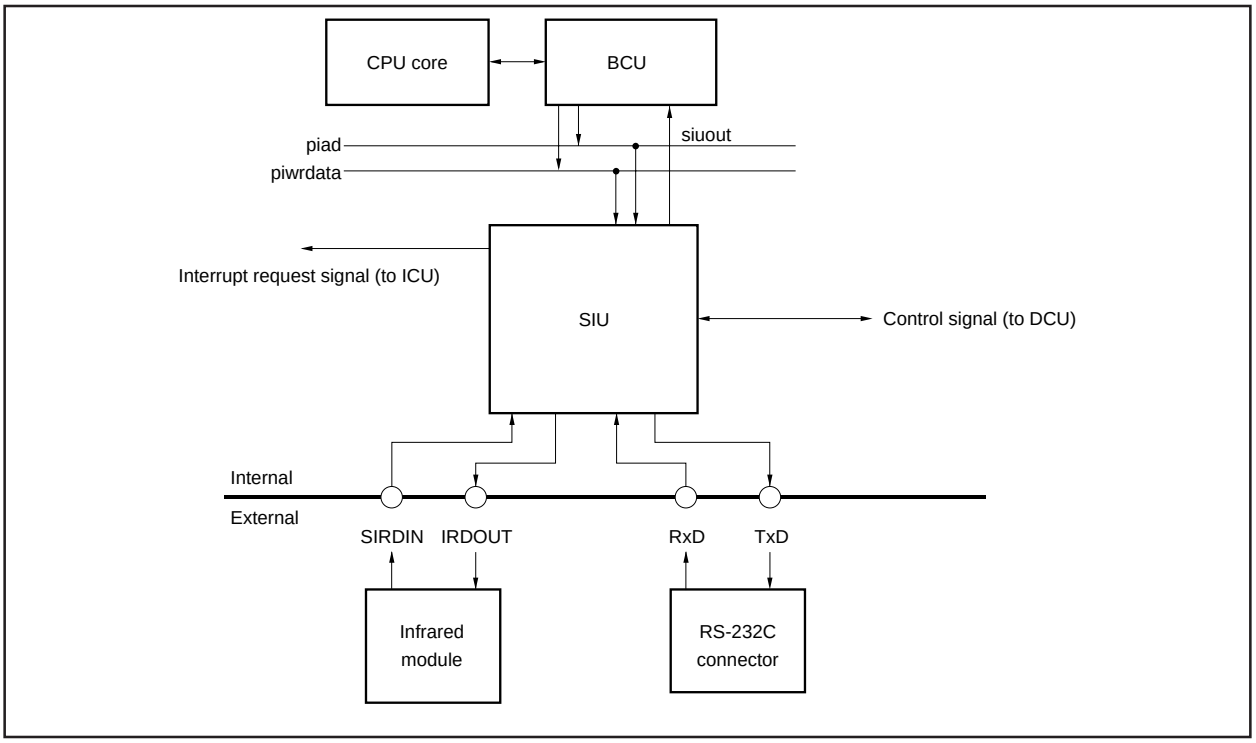
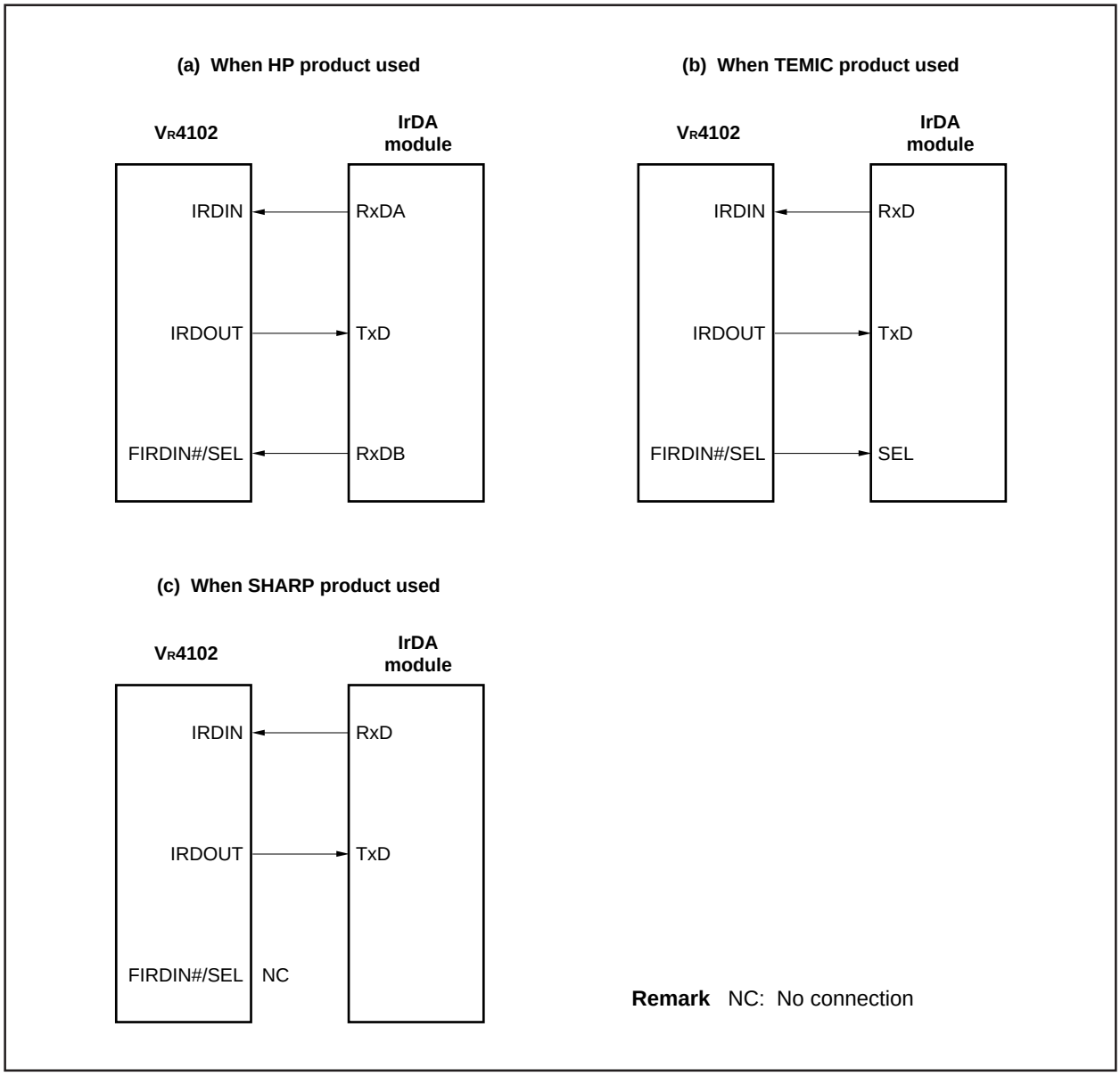


Figure 15-2. Connection Example between the VR4102 and IrDA Module



16. AIU (AUDIO INTERFACE UNIT)

16.1 General

AIU supports speaker output and MIC input operations. It has 10-bit A/D and D/A converters, and functions as the digital voice I/O interface. DMA operation is supported for both input and output operations.

Table 16-1. AIU Registers

Physical Address	Symbol	Function
0x0B00 0160	MDMADATREG	Mic input DMA data register
0x0B00 0162	SDMADATREG	Speaker output DMA data register
0x0B00 0166	SODATREG	Speaker output data register
0x0B00 0168	SCNTREG	Speaker output control register
0x0B00 016A	SCNVRREG	D/A conversion rate setting register
0x0B00 0170	MIDATREG	Mic input data register
0x0B00 0172	MCNTREG	Mic input control register
0x0B00 0174	MCNVRREG	A/D conversion rate setting register
0x0B00 0178	DVALIDREG	Data valid indicate register
0x0B00 017A	SEQREG	Sequencer operation enable register
0x0B00 017C	INTREG	AIU interrupt register

17. KIU (KEYBOARD INTERFACE UNIT)

17.1 General

KIU includes 12 scan lines and 8 detection lines to enable detection when any one of the 96 keys is pressed. The number of scan lines can be selected from 8, 10, and 12.

The 12 scan lines can be used as a general-purpose output port by setting the following registers.

Table 17-1. KIU Registers

Physical Address	Symbol	Function
0x0B00 0180	KIUDAT0	KIU data 0 register
0x0B00 0182	KIUDAT1	KIU data 1 register
0x0B00 0184	KIUDAT2	KIU data 2 register
0x0B00 0186	KIUDAT3	KIU data 3 register
0x0B00 0188	KIUDAT4	KIU data 4 register
0x0B00 018A	KIUDAT5	KIU data 5 register
0x0B00 0190	KIUSCANREP	KIU key scan control register
0x0B00 0192	KIUSCANS	KIU sequencer status register
0x0B00 0194	KIUWKS	KIU key scan wait time setting register
0x0B00 0196	KIUWKI	KIU key scan interval setting register
0x0B00 0198	KIUINT	KIU interrupt register
0x0B00 019A	KIURST	KIU reset register
0x0B00 019C	KIUGPEN	KIU general-purpose output enable register
0x0B00 019E	SCANLINE	KIU scan line control register

18. DebugSIU (DEBUG SERIAL INTERFACE UNIT)

18.1 General

The DebugSIU is a dedicated serial interface unit that is used during debugging. It supports a data transfer rate of up to 115 kbps. In addition to the DDIN and DDOUT I/O pins, it supports the DCTS# and DRTS# pins that are used for hardware flow control. These pins can be used as a general-purpose output port when DSIU is not used.

Table 18-1. DSIU Registers

Physical Address	Symbol	Function
0x0B00 01A0	PORTREG	General-purpose port switch register
0x0B00 01A2	MODEMREG	Modem control register
0x0B00 01A4	ASIM00REG	Asynchronous mode 0 register
0x0B00 01A6	ASIM01REG	Asynchronous mode 1 register
0x0B00 01A8	RXB0RREG	Extend receive buffer register
0x0B00 01AA	RXB0LREG	Receive buffer register
0x0B00 01AC	TXS0RREG	Extend transmit shift register
0x0B00 01AE	TXS0LREG	Transmit shift register
0x0B00 01B0	ASIS0REG	Communication state register
0x0B00 01B2	INTR0REG	DSIU interrupt register
0x0B00 01B6	BPRM0REG	Baud rate generator prescaler mode register
0x0B00 01B8	DSIURESETREG	DSIU reset register

19. LED (LED CONTROL UNIT)

19.1 General

LED switches LEDs on and off at a regular interval. This operation can be executed during standby, suspend, or hibernate mode, and the interval time can be programmed.

Table 19-1. LED Registers

Physical Address	Symbol	Function
0x0B00 0240	LEDHTSREG	LED ON time setting register
0x0B00 0242	LEDLTSREG	LED OFF time setting register
0x0B00 0248	LEDCNTREG	LED control register
0x0B00 024A	LEDASTCREG	LED auto stop time setting register
0x0B00 024C	LEDINTREG	LED interrupt register

20. HSP (MODEM INTERFACE UNIT)

20.1 General

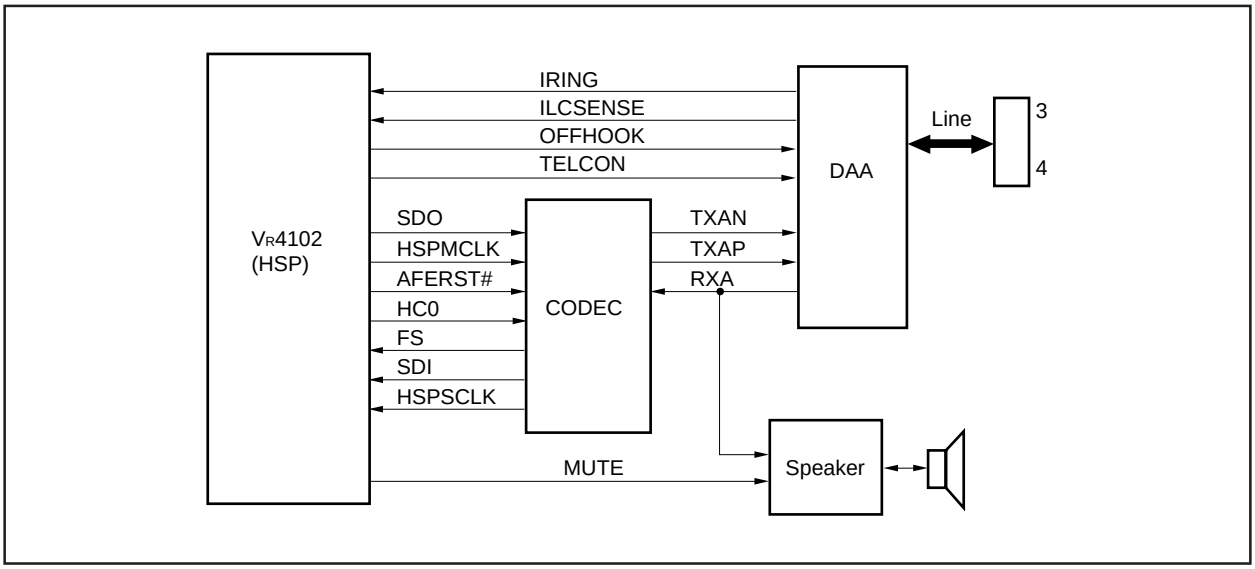
HSP performs interfaces between modem software and external circuits, for the CPU core. This unit uses PCtel's PCT288I, and it has the following main functions.

- Controls CODEC devices and performs serial/parallel conversion of CODEC transmitted/received data
- Controls signal lines in the data access arrangement block (DAA), such as relay or hook

Table 20-1. HSP Registers

Physical Address	R/W	Symbol	Function
0x0C00 0020	R/W	HSPINIT	HSP initialization register
0x0C00 0022	R/W	HSPDATA (7:0)	HSP data register (low-order)
0x0C00 0023	R/W	HSPDATA (15:8)	HSP data register (high-order)
0x0C00 0024	W	HSPINDEX	HSP index register
0x0C00 0028	R	HSPID (7:0)	HSP ID register
0x0C00 0029	R	HSPPCS (7:0)	HSP I/O address program confirmation register
	W	HSPPCTEL (7:0)	HSP signature check port

Figure 20-1. Block Connection Example



21. FIR (Fast IrDA INTERFACE UNIT)

21.1 General

FIR supports the IrDA 1.1 high-speed infrared ray communication physical layer standard. For infrared communication corresponding to IrDA 1.0, use SIU instead.

Table 21-1. FIR Registers

Physical Address	Symbol	Function
0x0C00 0040	FRSTR	FIR reset register
0x0C00 0042	DPINTR	DMA page interrupt register
0x0C00 0044	DPCNTR	DMA page control register
0x0C00 0050	TDR	Transmitted data register
0x0C00 0052	RDR	Received data register
0x0C00 0054	IMR	Interrupt mask register
0x0C00 0056	FSR	FIFO set-up register
0x0C00 0058	IRSR1	IR set-up register 1
0x0C00 005C	CRCSR	CRC set-up register
0x0C00 005E	FIRCR	FIR control register
0x0C00 0060	MIRCR	MIR control register
0x0C00 0062	DMACR	DMA control register
0x0C00 0064	DMAER	DMA enable register
0x0C00 0066	TXIR	Transmission indication register
0x0C00 0068	RXIR	Reception indication register
0x0C00 006A	IFR	Interrupt flag register
0x0C00 006C	RXSTS	Reception status register
0x0C00 006E	TXFL	Transmission frame length register L
0x0C00 0070	MRXF	Maximum reception flame length register
0x0C00 0074	RXFL	Reception frame length register L

22. INSTRUCTION SET

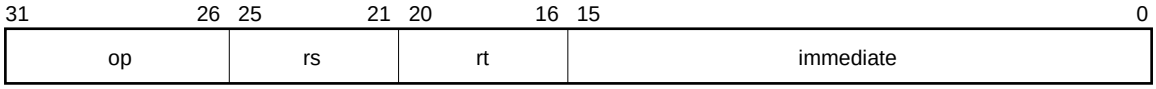
Each instruction of the VR4102 consists of 1 word (32 bits) located at a word boundary. Three instruction formats are available as shown in Figure 22-1. By employing the three simplified instruction formats, the decoding of instructions is simplified. Complicated operations and addressing modes that are not frequently used are realized by the compiler.

22.1 Instruction Formats

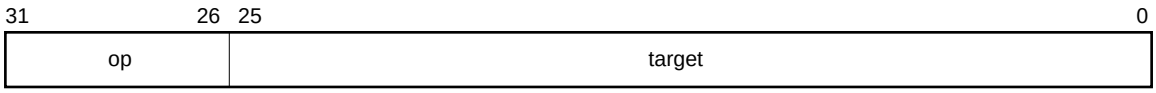
The instruction formats of the VR4102 are shown below.

Figure 22-1. CPU Instruction Format

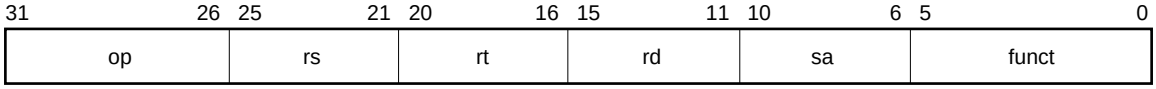
I-type (immediate format)



J-type (jump format)



R-type (register format)



op	6-bit instruction code
rs	5-bit source register specifier
rt	5-bit target (source/destination) register, or conditional branch
immediate	16-bit immediate value, branch off-set value, or address off-set value
target	26-bit branch destination address
rd	5-bit destination register specifier
sa	5-bit shift
funct	6-bit function field

22.2 CPU Instruction Set List

All the CPU instructions of the VR4102 are classified into three sets: instruction set common to all the VR Series processors (ISA: Instruction Set Architecture), instruction set executed by the VR4000 Series (extended ISA), and system control coprocessor instruction set. Each instruction set is listed below.

Table 22-1. CPU Instruction Set: ISA (1/2)

Instruction	Description	Format
Load/store instruction	op | base | rt | offset	
LB	Load Byte	LB rt, offset (base)
LBU	Load Byte Unsigned	LBU rt, offset (base)
LH	Load Halfword	LH rt, offset (base)
LHU	Load Halfword Unsigned	LHU rt, offset (base)
LW	Load Word	LW rt, offset (base)
LWL	Load Word Left	LWL rt, offset (base)
LWR	Load Word Right	LWR rt, offset (base)
SB	Store Byte	SB rt, offset (base)
SH	Store Halfword	SH rt, offset (base)
SW	Store Word	SW rt, offset (base)
SWL	Store Word Left	SWL rt, offset (base)
SWR	Store Word Right	SWR rt, offset (base)
AIU immediate instruction	op | rs | rt | offset	
ADDI	Add Immediate	ADDI rt, rs, immediate
ADDIU	Add Immediate Unsigned	ADDIU rt, rs, immediate
SLTI	Set On Less Than Immediate	SLTI rt, rs, immediate
SLTIU	Set On Less Than Immediate Unsigned	SLTIU rt, rs, immediate
ANDI	And Immediate	ANDI rt, rs, immediate
ORI	Or Immediate	ORI rt, rs, immediate
XORI	Exclusive Or Immediate	XORI rt, rs, immediate
LUI	Load Upper Immediate	LUI rt, immediate
3-operand type instruction	op | rs | rt | rd | sa | funct	
ADD	Add	ADD rd, rs, rt
ADDU	Add Unsigned	ADDU rd, rs, rt
SUB	Subtract	SUB rd, rs, rt
SUBU	Subtract Unsigned	SUBU rd, rs, rt
SLT	Set On Less Than	SLT rd, rs, rt
SLTU	Set On Less Than Unsigned	SLTU rd, rs, rt
AND	And	AND rd, rs, rt
OR	Or	OR rd, rs, rt
XOR	Exclusive Or	XOR rd, rs, rt
NOR	Nor	NOR rd, rs, rt
Shift instruction	op | rs | rt | rd | sa | funct	
SLL	Shift Left Logical	SLL rd, rt, sa
SRL	Shift Right Logical	SRL rd, rt, sa
SRA	Shift Right Arithmetic	SRA rd, rt, sa
SLLV	Shift Left Logical Variable	SLLV rd, rt, rs
SRLV	Shift Right Logical Variable	SRLV rd, rt, rs
SRAV	Shift Right Arithmetic Variable	SRAV rd, rt, rs

Table 22-1. CPU Instruction Set: ISA (2/2)

Instruction	Description	Format
Multiplication/division instruction	op | rs | rt | rd | sa | funct	
MULT	Multiply	MULT rs, rt
MULTU	Multiply Unsigned	MULTU rs, rt
DIV	Divide	DIV rs, rt
DIVU	Divide Unsigned	DIVU rs, rt
MFHI	Move From HI	MFHI rd
MFLO	Move From LO	MFLO rd
MTHI	Move To HI	MTHI rs
MTLO	Move To LO	MTLO rs
Jump instruction (1)	op | target	
J	Jump	J target
JAL	Jump And Link	JAL target
Jump instruction (2)	op | rs | rt | rd | sa | funct	
JR	Jump Register	JR rs
JALR	Jump And Link Register	JALR rs, rd
Branch instruction (1)	op | rs | rt | offset	
BEQ	Branch On Equal	BEQ rs, rt, offset
BNE	Branch On Not Equal	BNE rs, rt, offset
BLEZ	Branch On Less Than Or Equal To Zero	BLEZ rs, offset
BGTZ	Branch On Greater Than Zero	BGTZ rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset	
BLTZ	Branch On Less Than Zero	BLTZ rs, offset
BGEZ	Branch On Greater Than Or Equal to Zero	BGEZ rs, offset
BLTZAL	Branch On Less Than Zero And Link	BLTZAL rs, offset
BGEZAL	Branch On Greater Than Or Equal To Zero And Link	BGEZAL rs, offset
Special instruction	SPECIAL | rs | rt | rd | sa | funct	
SYNC	Synchronize	SYNC
SYSCALL	System Call	SYSCALL
BREAK	Breakpoint	BREAK
Coprocessor instruction (1)	op | rs | rt | rd | sa | funct	
LWCz	Load Word To Coprocessor z	LWCz rt, offset (base)
SWCz	Store Word From Coprocessor z	SWCz rt, offset (base)
Coprocessor instruction (2)	op | rs | rt | rd | sa | funct	
MTCz	Move To Coprocessor z	MTCz rt, rd
MFCz	Move From Coprocessor z	MFCz rt, rd
CTCz	Move Control To Coprocessor z	CTCz rt, rd
CFCz	Move Control From Coprocessor z	CFCz rt, rd
Coprocessor instruction (3)	COPz | CO | cofun	
COPz	Coprocessor z Operation	COPz cofun
Coprocessor instruction (4)	COPz | BC | br | offset	
BCzT	Branch On Coprocessor z True	BCzT offset
BCzF	Branch On Coprocessor z False	BCzF offset

Table 22-2. CPU Instruction Set: Extended ISA (1/2)

Instruction	Description	Format
Load/store instruction	op | base | rt | offset	
LD	Load Doubleword	LD rt, offset (base)
LDL	Load Doubleword Left	LDL rt, offset (base)
LDR	Load Doubleword Right	LDR rt, offset (base)
LWU	Load Word Unsigned	LWU rt, offset (base)
SD	Store Doubleword	SD rt, offset (base)
SDL	Store Doubleword Left	SDL rt, offset (base)
SDR	Store Doubleword Right	SDR rt, offset (base)
AIU immediate instruction	op | rs | rt | immediate	
DADDI	Doubleword Add Immediate	DADDI rt, rs, immediate
DADDIU	Doubleword Add Immediate Unsigned	DADDIU rt, rs, immediate
3-operand type instruction	op | rs | rt | rd | sa | funct	
DADD	Doubleword Add	DADD rd, rs, rt
DADDU	Doubleword Add Unsigned	DADDU rd, rs, rt
DSUB	Doubleword Subtract	DSUB rd, rs, rt
DSUBU	Doubleword Subtract Unsigned	DSUBU rd, rs, rt
Shift instruction	op | rs | rt | rd | sa | funct	
DSLL	Doubleword Shift Left Logical	DSLL rd, rt, sa
DSRL	Doubleword Shift Right Logical	DSRL rd, rt, sa
DSRA	Doubleword Shift Right Arithmetic	DSRA rd, rt, sa
DSLLV	Doubleword Shift Left Logical Variable	DSLLV rd, rt, rs
DSRLV	Doubleword Shift Right Logical Variable	DSRLV rd, rt, rs
DSRAV	Doubleword Shift Right Arithmetic Variable	DSRAV rd, rt, rs
DSLL32	Doubleword Shift Left Logical+32	DSLL32 rd, rt, sa
DSRL32	Doubleword Shift Right Logical+32	DSRL32 rd, rt, sa
DSRA32	Doubleword Shift Right Arithmetic+32	DSRA32 rd, rt, sa
Multiplication/division instruction (1)	op | rs | rt | rd | sa | funct	
DMULT	Doubleword Multiply	DMULT rs, rt
DMULTU	Doubleword Multiply Unsigned	DMULTU rs, rt
DDIV	Doubleword Divide	DDIV rs, rt
DDIVU	Doubleword Divide Unsigned	DDIVU rs, rt
Multiplication/division instruction (2)	op | rs | rt | immediate	
MADD16	Multiply and Add 16-bit Integer	MADD16 rs, rt
DMADD16	Doubleword Multiply and Add 16-bit Integer	DMADD16 rs, rt
Branch instruction (1)	op | rs | rt | offset	
BEQL	Branch On Equal Likely	BEQL rs, rt, offset
BNEL	Branch On Not Equal Likely	BNEL rs, rt, offset
BLEZL	Branch On Less Than Or Equal To Zero Likely	BLEZL rs, offset
BGTZL	Branch On Greater Than Zero Likely	BGTZL rs, offset

Table 22-2. CPU Instruction Set: Extended ISA (2/2)

Instruction	Description	Format
Branch instruction (2)	REGIMM | rs | sub | offset	
BLTZL	Branch On Less Than Zero Likely	BLTZL rs, offset
BGEZL	Branch On Greater Than Or Equal To Zero Likely	BGEZL rs, offset
BLTZALL	Branch On Less Than Zero And Link Likely	BLTZALL rs, offset
BGEZALL	Branch On Greater Than Or Equal To Zero And Link Likely	BGEZALL rs, offset
Exception instruction	SPECIAL | rs | rt | rd | sa | funct	
TGE	Trap If Greater Than Or Equal	TGE rs, rt
TGEU	Trap If Greater Than Or Equal Unsigned	TGEU rs, rt
TLT	Trap If Less Than	TLT rs, rt
TLTU	Trap If Less Than Unsigned	TLTU rs, rt
TEQ	Trap If Equal	TEQ rs, rt
TNE	Trap If Not Equal	TNE rs, rt
Exception immediate instruction	REGIMM | rs | sub | immediate	
TGEI	Trap If Greater Than Or Equal Immediate	TGEI rs, immediate
TGEIU	Trap If Greater Than Or Equal Immediate Unsigned	TGEIU rs, immediate
TLTI	Trap If Less Than Immediate	TLTI rs, immediate
TLTIU	Trap If Less Than Immediate Unsigned	TLTIU rs, immediate
TEQI	Trap If Equal Immediate	TEQI rs, immediate
TNEI	Trap If Not Equal Immediate	TNEI rs, immediate

Table 22-3. System Control Coprocessor (CP0) Instruction Set

Instruction	Description	Format
System control coprocessor instruction (1)	COP0 | sub | rt | rd | 0	
MFC0	Move From Coprocessor 0	MFC0 rt, rd
MTC0	Move To Coprocessor 0	MTC0 rt, rd
DMFC0	Doubleword Move From Coprocessor 0	DMFC0 rt, rd
DMTC0	Doubleword Move To Coprocessor 0	DMTC0 rt, rd
System control coprocessor instruction (2)	COP0 | CO | funct	
TLBR	Read Indexed TLB Entry	TLBR
TLBWI	Write Indexed TLB Entry	TLBWI
TLBWR	Write Random TLB Entry	TLBWR
TLBP	Probe TLB For Matching Entry	TLBP
ERET	Exception Return	ERET
System control coprocessor instruction (3)	COP0 | CO | funct	
STANDBY	Standby	STANDBY
SUSPEND	Suspend	SUSPEND
HIBERNATE	Hibernate	HIBERNATE
System control coprocessor instruction (4)	CACHE | base | sub | offset	
CACHE	Cache Operation	CACHE sub, offset (base)

22.3 Instruction Execution Time

In principle, the VR4102 executes one instruction in one cycle, but some instructions take two cycles or more.

(1) The data loaded by a load instruction cannot be used in the delay slot. If an instruction that uses load data is placed in the delay slot, the pipeline stalls.
A store instruction stalls by the delay slot if it is followed by a load instruction or MFC0.
If a branch instruction whose condition is satisfied or a jump instruction is executed, the instruction at the destination address is executed after the delay slot.

Table 22-4. Number of Delay Slot Cycles

Instruction Category	Necessary Number of Cycles (PCycle)
Load	1
Store	1
Jump	1
Branch	1

(2) The number of cycles indicated in the table below is necessary for executing an integer multiplication/division or sum-of-products operation instruction.
These instructions can be executed in parallel with other instructions, except those that access the HI/LO registers that store the result of an operation, and multiplication/division or sum-of-products operation instruction.

Table 22-5. Number of Execution Cycles of Integer Multiplication/Division Instructions

Instruction Category	Necessary Number of Cycles (PCycle)
MULT	1
MULTU	1
DIV	35
DIVU	35
DMULT	4
DMULTU	4
DDIV	67
DDIVU	67
MADD16	1
DMADD16	1

23. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}		–0.5 to +4.0	V
Input voltage	V_I	$V_{DD} \geq 3.7$ V	–0.5 to +4.0	V
		$V_{DD} < 3.7$ V	–0.5 to V_{DD} + 0.3	V
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.

The specifications and conditions shown in DC Characteristics and AC Characteristics are the ranges for normal operation and quality assurance of the product.

3. V_I can be –1.5 V if the input pulse is less than 10 ns.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHZ		10	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.		10	pF

DC Characteristics (T_A = –10 to +70°C, V_{DD} = 3.0 to 3.6 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = –2 mA	0.8V_{DD}			V
		I_{OH} = –20 μA	V_{DD} – 0.1			
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
		I_{OL} = 20 μA			0.1	
High-level input voltage[Note 1]	V_{IH1}		2.0		V_{DD} + 0.3	V
Low-level input voltage[Note 1]	V_{IL1}		–0.3		0.3V_{DD}	V
		Pulse less than 10 ns	–1.5		0.3V_{DD}	V
High-level input voltage[Note 2]	V_{IH2}		0.75V_{DD}		V_{DD} + 0.3	V
Low-level input voltage[Note 2]	V_{IL2}		–0.3		0.6	V
		Pulse less than 10 ns	–1.5		0.6	V
Hysteresis voltage[Note 3]	V_H			0.17V_{DD}		V
Supply current[Note 4]	I_{DD}	ADD (0:25), RD#, WR#, TPX (0:1), TPY (0:1) = 120 pF, Other pins = 40 pF, In Fullspeed mode		108	Under evaluation (237.5)	mA
		External load: 0 pF, in Standby mode		50	95	
		External load: 0 pF, in Suspend mode		10	15	
		External load: 0 pF, in Hibernate mode, when LED unit is off.		100	200	μA
Input leakage current[Note 4]	I_{LI}	V_{DD} = 3.6 V, V_I = V_{DD}, 0 V			±5	μA
High-level input leakage current[Note 5]	I_{LIH}	V_{DD} = 3.6 V, V_I = V_{DD}			36	μA
Output leakage current	I_{LO}	V_{DD} = 3.6 V, V_I = V_{DD}, 0 V			±5	μA

Notes 1. Except RTCX1, CLKX1, FIRCLK, HSPSCLK, TPX (0:1), TPY (0:1), ADIN (0:2), AUDIOIN, POWER, RSTSW#, RTCRST#, GPIO (0:3), GPIO (9:12), BATTINH/BATTINT#, IRING, and KPORT (0:7) pins

2. Applied to POWER, RSTSW#, RTCRST#, GPIO (0:3), GPIO (9:12), BATTINH/BATTINT#, IRING, and KPORT (0:7) pins

3. Hysteresis voltage: Difference between the minimum voltage at which the high level of a Schmitt input signal is not recognized when the signal goes from low to high and the maximum voltage at which the low level is not recognized when the signal goes from high to low

4. Except KPORT (0:7) (input pins with pull-down resistor)

5. Applied to KPORT (0:7) (input pins with pull-down resistor)

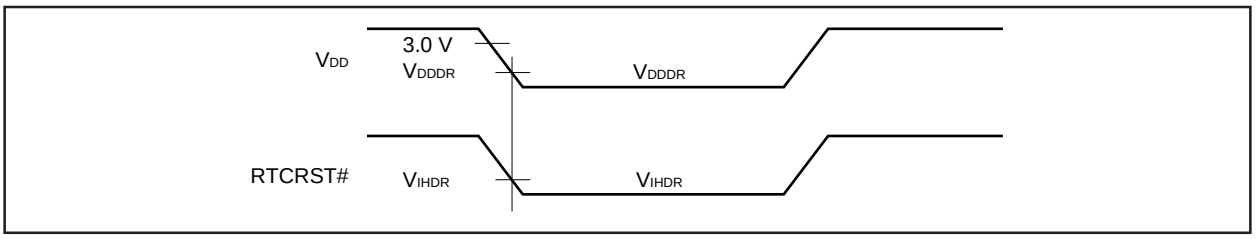
Data Retention Characteristics (T_A = 25°C)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data retention voltage[Note 1]	V_{DDDR}	Hibernate mode	2.5	3.6	V
Data retention high-level input voltage[Note 2]	V_{IHDR}		Under evaluation ($0.9V_{DDDR}$)		V

Notes 1. The data retention voltage guarantees retention of the data read from the following registers for the RTC operation, and the data of the compare register (the data in the CPU core cannot be guaranteed).
ETIMELREG, ETIMEMREG, ETIMEHREG, ECOMPLREG, ECOMPMREG, ECOMPHREG

2. Applied to RTCRST# pin

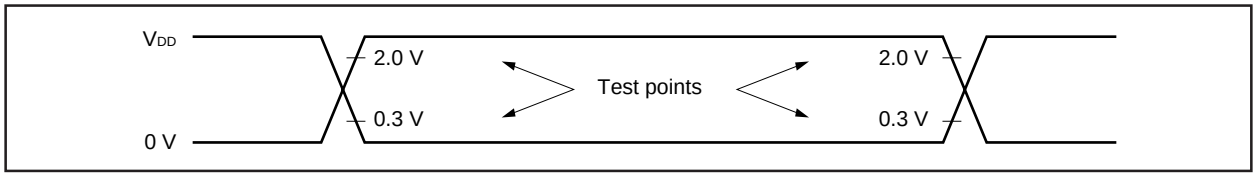
Remark The values in parentheses are the targeted values.



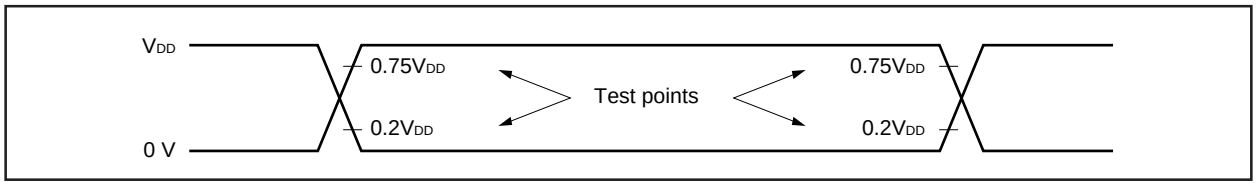
AC Characteristics (T_A = –10 to +70°C, V_{DD} = 3.0 to 3.6 V)

AC test input waveform

(a) CTS#, DATA (0:15), DATA (16:31)/GPIO (16:31), DBUS32/GPIO48, DCD#/GPIO15, DCTS#/GPIO47, DDIN/GPIO45, DSR#, DTR#/CLKSEL0, FS, FIRDIN#SEL, GPIO49, GPIO (4:8), HLDRQ#, ILCSENSE, IOCHRDY, IOCS16#, IRDIN, LCDRDY, MEMCS16#, RxD, RTS#/CLKSEL1, SDI, TxD/CLKSEL2, ZWS#

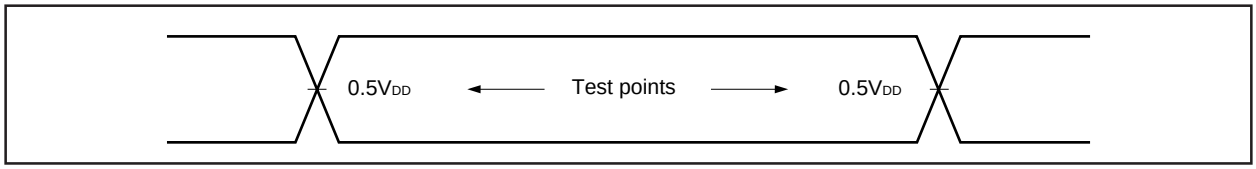


(b) BATTINH/BATTINT#, GPIO (0:3), GPIO (9:12), IRING, KPORT (0:7), POWER, RSTSW#, RTCRST#



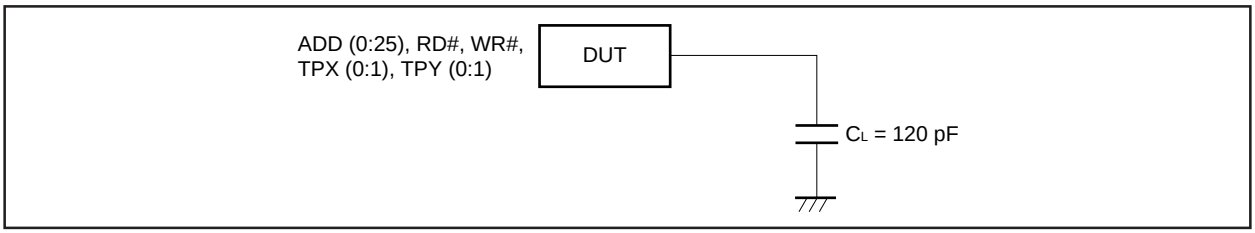
AC test output measuring points

(c) ADD (0:25), AFERST#, BUSCLK, GPIO49, DATA (0:15), DATA (16:31)/GPIO (16:31), DBUS32/GPIO48, DCTS#/GPIO47, DDIN/GPIO45, DDOUT/GPIO44, DRTS#/GPIO46, DTR#/CLKSEL0, FIRDIN#/SEL, GPIO (0:14), HC0, HLDACK#, HSPMCLK, IOR#, IOW#, IRDOUT#, KSCAN (0:11)/GPIO (32:43), LCAS#, LCDCS#, LEDOUT#, MEMR#, MEMW#, MPOWER, MRAS (0:1)#, MUTE, OFFHOOK, OPD#, POWERON, RD#, ROMCS (0:3)#, RSTOUT, RTS#/CLKSEL1, SDO, SHB#, TELCON, TPX (0:1), TPY (0:1), TxD/CLKSEL2, UCAS#, ULCAS#/MRAS2#, UUCAS#/MRAS3#, WR#

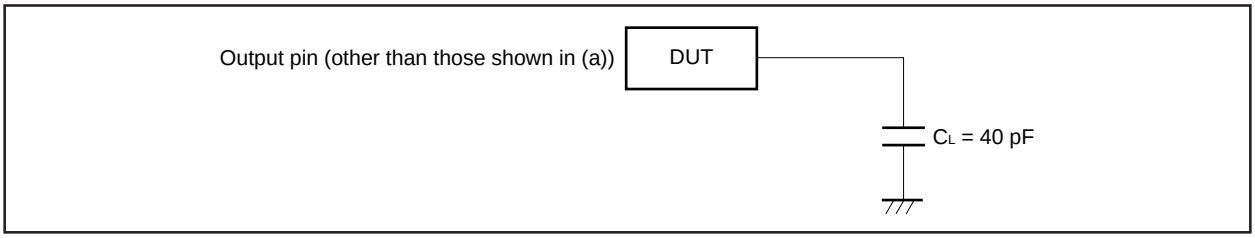


Load condition

(a) ADD (0:25), RD#, WR#, TPX (0:1), TPY (0:1)



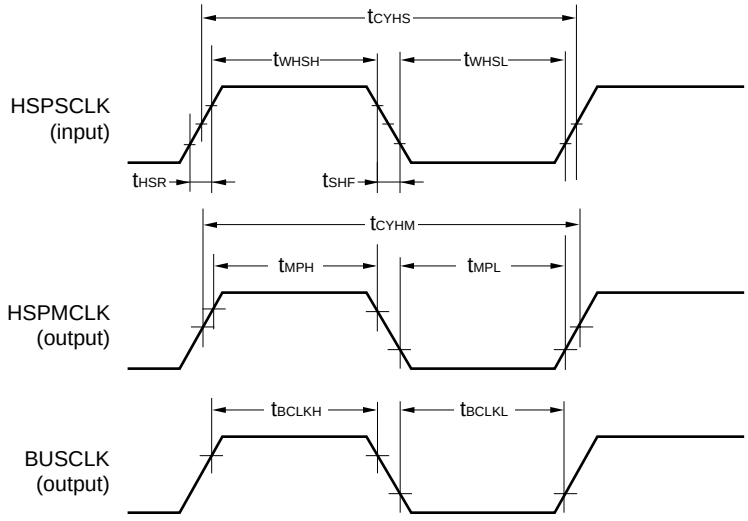
(b) Other output pins



(1) Clock parameter

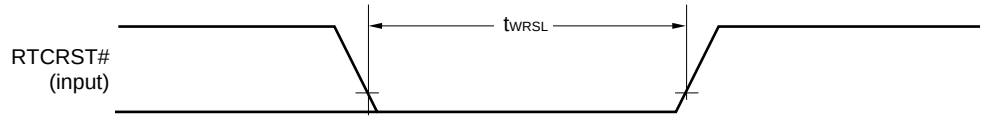
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
HSPSCLK high-level width	t_{WHSH}	When HSP unit is used	40			ns
HSPSCLK low-level width	t_{WHSL}	When HSP unit is used	40			ns
HSPSCLK clock frequency	t_{HSCYC}	When HSP unit is used			t_{MCYC}	MHz
HSPSCLK clock cycle	t_{CYHS}	When HSP unit is used	108.5			ns
HSPSCLK clock rise time	t_{HSR}	When HSP unit is used			10	ns
HSPSCLK clock fall time	t_{SHF}	When HSP unit is used			10	ns
HSPMCLK high-level width	t_{MPH}	When HSP unit is used	$t_{CYHM} \times 0.45$		$t_{CYHM} \times 0.55$	ns
HSPMCLK low-level width	t_{MPL}	When HSP unit is used	$t_{CYHM} \times 0.45$		$t_{CYHM} \times 0.55$	ns
HSPMCLK clock frequency	t_{MCYC}	When HSP unit is used	0.585		18.432	MHz
HSPMCLK clock cycle	t_{CYHM}	When HSP unit is used	54.253		1790.365	ns
BUSCLK high-level width	t_{BCLKH}		45			ns
BUSCLK low-level width	t_{BCLKL}		45			ns
FIRCLK input frequency**Note**	t_{FIRCYC}	In FIR mode	47.996	48.000	48.005	MHz
		In MIR mode	47.952		48.048	
FIRCLK clock duty**Note**	$t_{FIRDUTY}$		42		58	%

Note Applied to FIRCLK pin.



(2) Reset parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	Applied to RTCRST# pin	305		μs



Caution For the RTCRST# characteristics at power supply, refer to VR4102 User's Manual.

(3) GPIO interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{INP1}	**Note 1**	91.5		μs
	t_{INP2}	**Note 2**	361.5		ns
	t_{INP3}	**Note 3**	180.6		ns
GPIO input rise time 1[Note 4]	t_{GPINR1}			200	ns
GPIO input fall time 1[Note 4]	t_{GPINF1}			200	ns
GPIO input rise time 2[Note 5]	t_{GPINR2}			10	ns
GPIO input fall time 2[Note 5]	t_{GPINF2}			10	ns
Output level width	t_{OUTP1}	**Note 6**	29		μs
	t_{OUTP2}	**Note 7**	60		ns
	t_{OUTP3}	**Note 8**	30		ns

Notes 1. Applied to GPIO (0:3) pins.

2. Applied to DCD#/GPIO15 and GPIO (9:14) pins.

3. Applied to DATA (16:31)/GPIO (16:31) and GPIO (4:8) pins.

4. Applied to GPIO (0:4) pins.

5. Applied to DATA (16:31)/GPIO (16:31), DCD#/GPIO15, and GPIO (5:14) pins.

6. Applied to GPIO (0:4) pins.

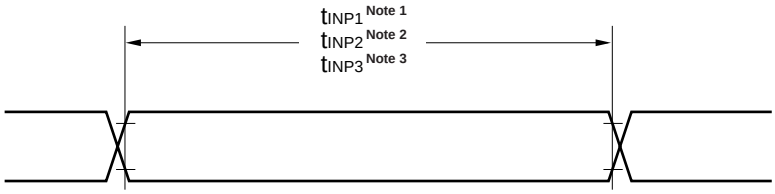
7. Applied to GPIO (9:14) pins.

8. Applied to GPIO (5:8), DATA (16:31)/GPIO (16:31), KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, and GPIO49 pins.

Caution These parameters are applied when the DATA (16:31)/GPIO (16:31), DCD#/GPIO15, KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, or GPIO49 pin is used as the GPIO pin.

(3) GPIO interface parameter (2/2)

(a) Input level width

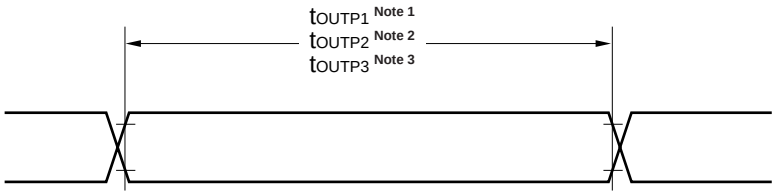


Notes 1. GPIO (0:3)
2. DCD#/GPIO15, GPIO (9:14)
3. DATA (16:31)/GPIO (16:31), GPIO (4:8)

(b) GPIO input rise/fall time

Notes 1. GPIO (0:4)
2. DATA (16:31)/GPIO (16:31), DCD#/GPIO15, GPIO (5:14)

(c) Output level width



Notes 1. GPIO (0:4)
2. GPIO (9:14)
3. GPIO (5:8), DATA (16:31)/GPIO (16:31), KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, GPIO49

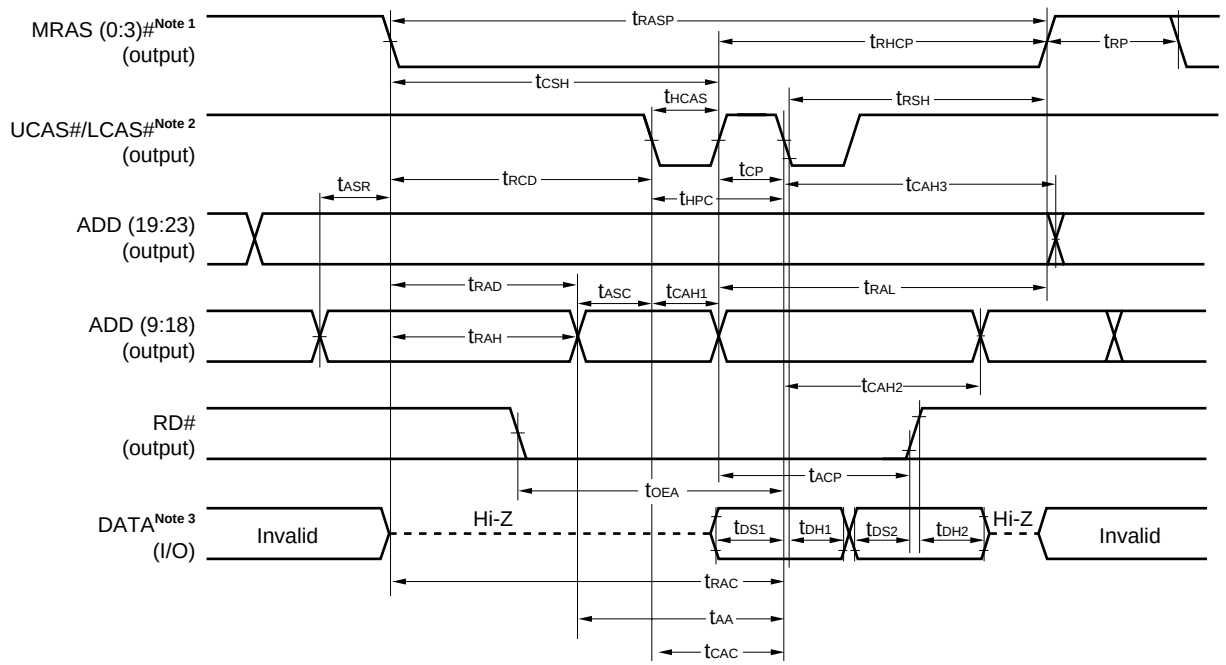
(4) EDO type DRAM parameter (1/3)

The target DRAM is the μPD42S16165L-A60, μPD42S18165L-A60, μPD42S64165G5-A50, or μPD42S64165G5-A60.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3)# pulse width	t_{RASP}		65		ns
MRAS (0:3)# hold time (from UCAS#/LCAS# precharge)	t_{RHCP}		40		ns
MRAS (0:3)# precharge time	t_{RP}		41		ns
UCAS#/LCAS# hold time (from UCAS#/LCAS#)	t_{CHS}		45		ns
UCAS#/LCAS# pulse width	t_{HCAS}		10		ns
UCAS#/LCAS# precharge time	t_{CP}		10		ns
Read/write cycle time	t_{HPC}		25		ns
MRAS (0:3)# hold time (from UCAS#/LCAS#)	t_{RSH}		20		ns
Row address setup time (to MRAS (0:3)#)	t_{ASR}		0		ns
UCAS#/LCAS# ↓ delay time from MRAS (0:3)# ↓	t_{RCD}		19		ns
Column address delay time from MRAS (0:3)# ↓	t_{RAD}		17		ns
Column address setup time (to UCAS#/LCAS#)	t_{ASC}		0		ns
Column address reference time (to MRAS (0:3)#)	t_{RAL}		35		ns
Row address hold time (from MRAS (0:3)#)	t_{RAH}		15		ns
Column address hold time 1 (from UCAS#/LCAS# ↓)	t_{CAH1}		10		ns
Column address hold time 2 (from UCAS#/LCAS# ↓)	t_{CAH2}		10		ns
Column address hold time 3 (from UCAS#/LCAS# ↓)	t_{CAH3}		10		ns
MRAS (0:3)# ↓ access time from UCAS#/LCAS# precharge	t_{ACP}		40		ns
RD# access time	t_{OEA}		20		ns
Data input setup time 1 (to UCAS#/LCAS# ↓)	t_{DS1}		0		ns
Data input hold time 1 (from MRAS (0:3)#)	t_{DH1}		6		ns
Data input setup time 2 (to UCAS#/LCAS# ↓)	t_{DS2}		0		ns
Data input hold time 2 (from MRAS (0:3)#)	t_{DH2}		6		ns
UCAS#/LCAS# ↓ access time from MRAS (0:3)# ↓	t_{RAC}		65		ns
UCAS#/LCAS# ↓ access time from column address	t_{AA}		31		ns
UCAS#/LCAS# ↓ access time from UCAS#/LCAS# ↓	t_{CAC}		20		ns
WR# setup time	t_{WCS}		0		ns
WR# hold time (from UCAS#/LCAS# ↓)	t_{WCH}		10		ns
Data delay 1	t_{D1}		0		ns
Data delay 2	t_{D2}		10		ns

Caution These ratings are applied only when a device operates within the recommended operating condition range and the operating ambient temperature is kept constant.
If the power supply voltage or operating ambient temperature changes during DRAM access, the above ratings are not applied.

(4) EDO type DRAM parameter (read parameter) (2/3)

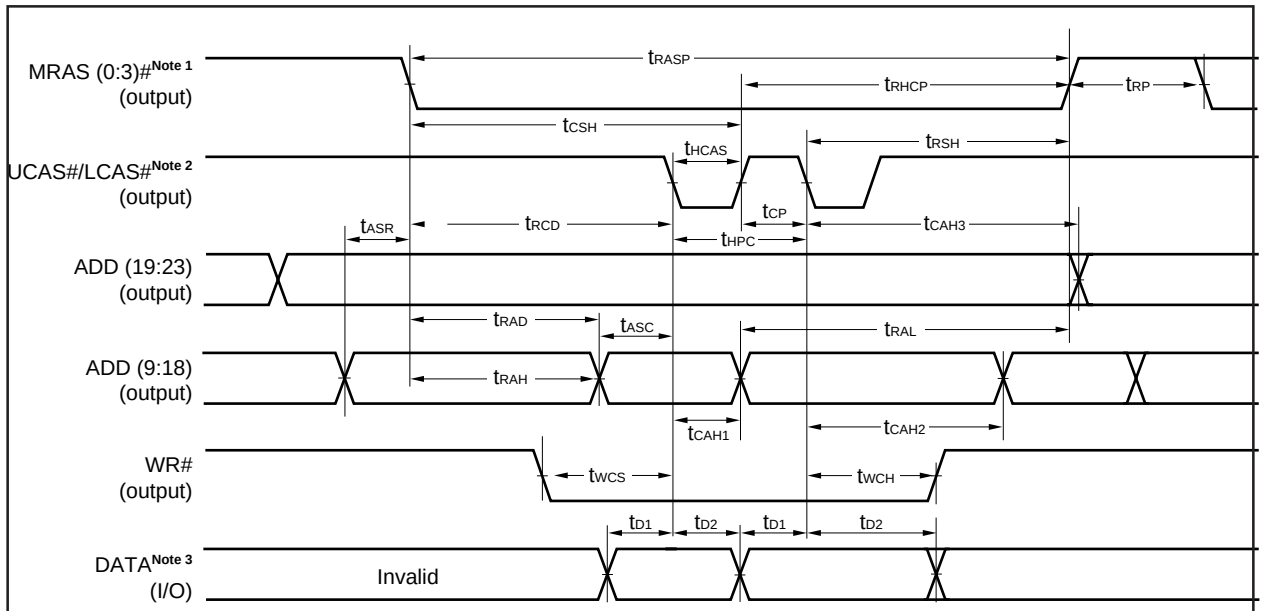


Notes 1. In 32-bit mode: MRAS (0:1)#
In 16-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, or MRAS (0:1)#

2. In 32-bit mode: UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, or LCAS#
In 16-bit mode: UCAS# or LCAS#

3. In 32-bit mode: DATA (16:31)/GPIO (16:31) or DATA (0:15)
In 16-bit mode: DATA (0:15)

(4) EDO type DRAM parameter (write parameter) (3/3)



Notes 1. In 32-bit mode: MRAS (0:1)#
In 16-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, or MRAS (0:1)#

2. In 32-bit mode: UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, or LCAS#
In 16-bit mode: UCAS# or LCAS#

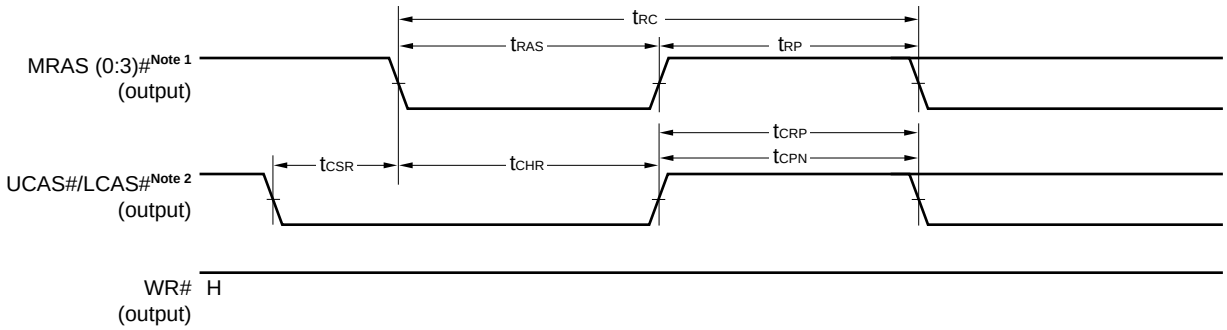
3. In 32-bit mode: DATA (16:31)/GPIO (16:31) or DATA (0:15)
In 16-bit mode: DATA (0:15)

(5) DRAM refresh parameter

The target DRAM is the μPD42S161615L-A60, μPD42S18165L-A60, μPD42S64165G5-A50, or μPD42S64165G5-A60

(a) CAS-before-RAS refresh parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Read/write cycle time	t_{RC}		104		ns
MRAS (0:3)# pulse width	t_{RAS}		60		ns
MRAS (0:3)# precharge time	t_{RP}		50		ns
UCAS#/LCAS# setup time (to MRAS (0:3)# ↓)	t_{CSR}		5		ns
UCAS#/LCAS# hold time (from MRAS (0:3)# ↓)	t_{CHR}		10		ns
MRAS (0:3)# precharge time from UCAS#/LCAS# ↑	t_{CRP}		5		ns
UCAS#/LCAS# precharge time	t_{CPN}		10		ns



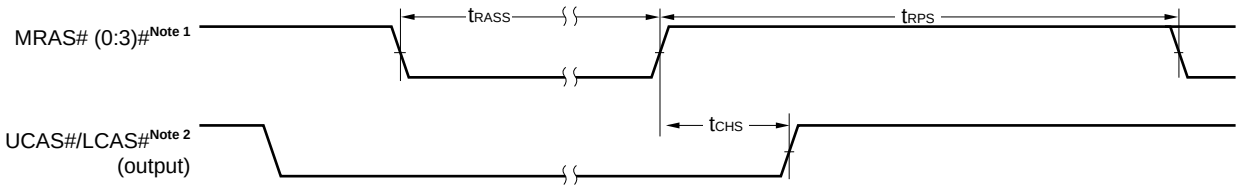
Notes 1. In 32-bit mode: MRAS (0:1)#
In 16-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, or MRAS (0:1)#

2. In 32-bit mode: UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, or LCAS#
In 16-bit mode: UCAS# or LCAS#

(b) CAS-before-RAS self-refresh parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3)# pulse width[Note]	t_{RASS}		100		μs
MRAS (0:3)# precharge time	t_{RPS}		110		ns
UCAS#/LCAS# hold time	t_{CHS}		–50		ns

Note The CAS-before-RAS self-refresh parameter is valid when t_{RASS} exceeds 100 μs.



Notes 1. In 32-bit mode: MRAS (0:1)#
In 16-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, or MRAS (0:1)#

2. In 32-bit mode: UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, or LCAS#
In 16-bit mode: UCAS# or LCAS#

(6) Normal ROM parameter

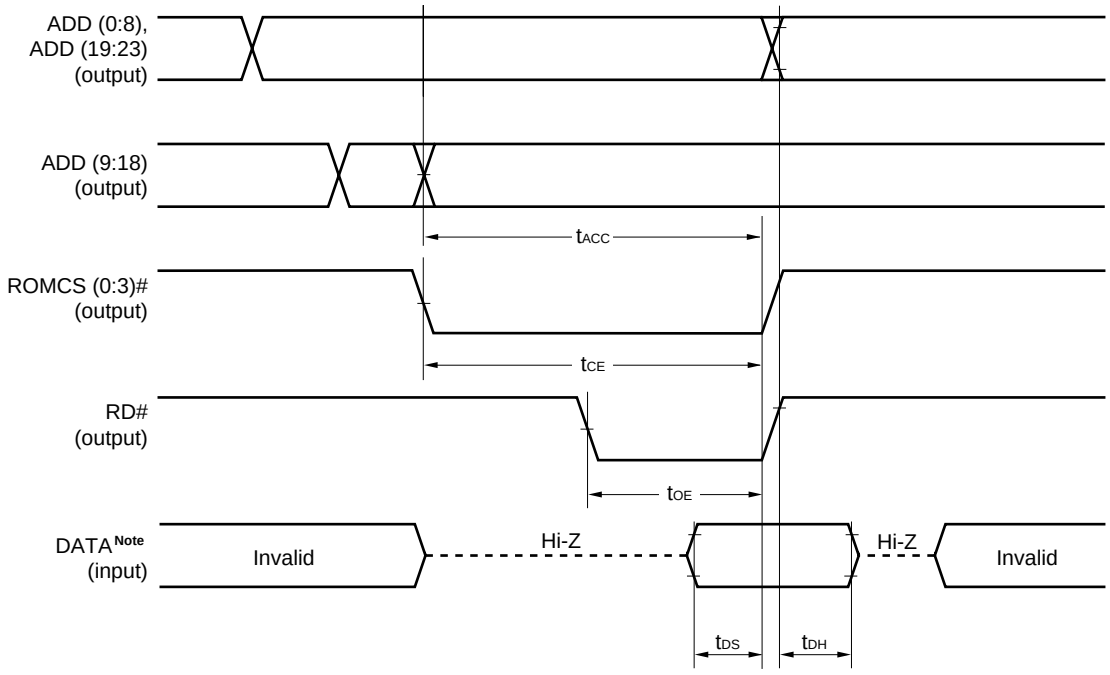
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Access time width from address[Note]	t_{ACC}		T x N – 19		ns
Access time width from ROMCS (0:3)#[Note]	t_{CE}		T x N – 19		ns
Access time width from RD#[Note]	t_{OE}		T x N – 28		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		6		ns

Note The value of N is set by using the WROMA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD#/CLKSEL2, RTS#CLKSEL1, and DTR#CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1	0	1	37.3
1	0	0	40.6

WROMA2	WROMA1	WROMA0	N
0	0	0	9
0	0	1	8
0	1	0	7
0	1	1	6
1	0	0	5
1	0	1	4
1	1	0	3
1	1	1	2

When WROMA (0 : 2) = 111B



Note In 32-bit mode: DATA (16:31)/GPIO (16:31) or DATA (0:15)
In 16-bit mode: DATA (0:15)

(7) Page ROM parameter

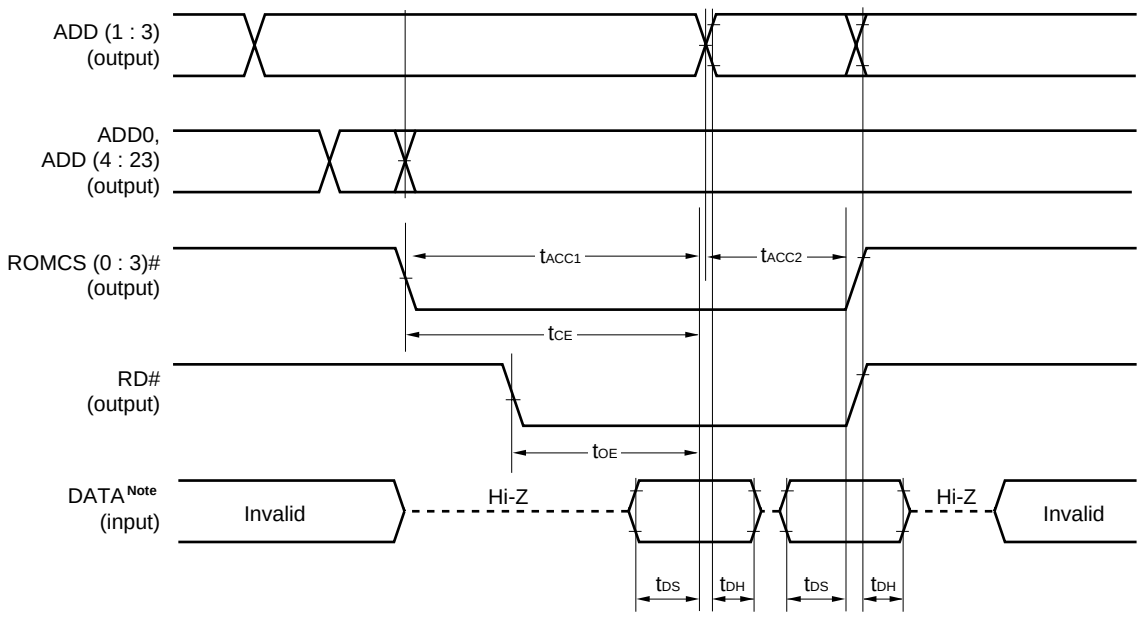
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Access time width 1 from address[Note]	t_{ACC1}		T x N – 19		ns
Access time width 2 from address[Note]	t_{ACC2}		T x N – 27		ns
Access time width from ROMCS (0:3)#[Note]	t_{CE}		T x N – 19		ns
Access time width from RD#[Note]	t_{OE}		T x N – 29		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		6		ns

Note The value of N is set by using the WROMA (0:2) bits of the BCUSPEEDREG register.
The value of M is set by using the WPROM (0:1) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD#/CLKSEL2, RTS#CLKSEL1, and DTR#CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1	0	1	37.3
1	0	0	40.6

WPROM1	WPROM0	M (TClock)
0	0	3
0	1	2
1	0	1
1	1	–

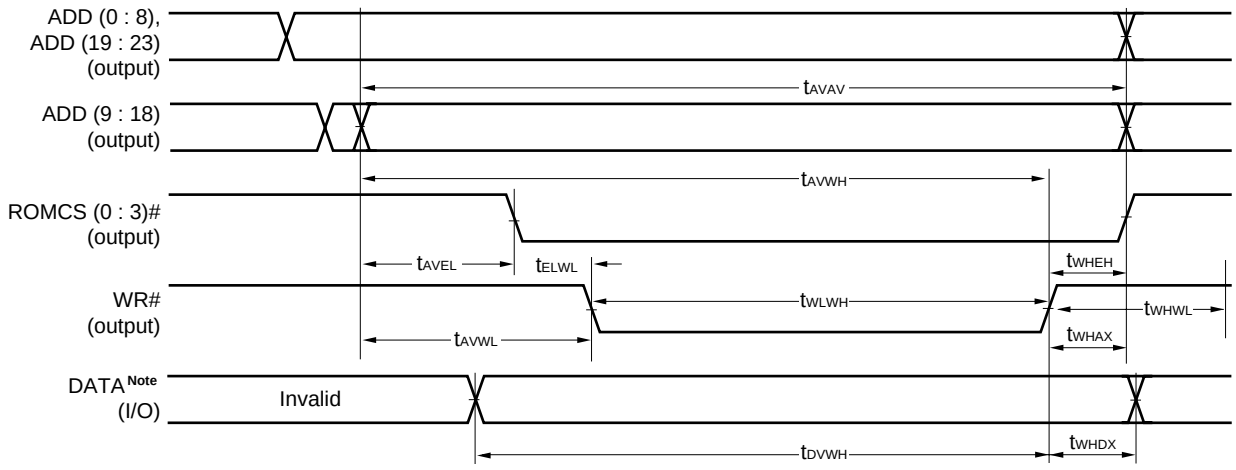
WROMA2	WROMA1	WROMA0	N (TClock)
0	0	0	9
0	0	1	8
0	1	0	7
0	1	1	6
1	0	0	5
1	0	1	4
1	1	0	3
1	1	1	2



Note In 32-bit mode: DATA (16:31)/GPIO (16:31) or DATA (0:15)
In 16-bit mode: DATA (0:15)

(8) Flash memory mode write parameter

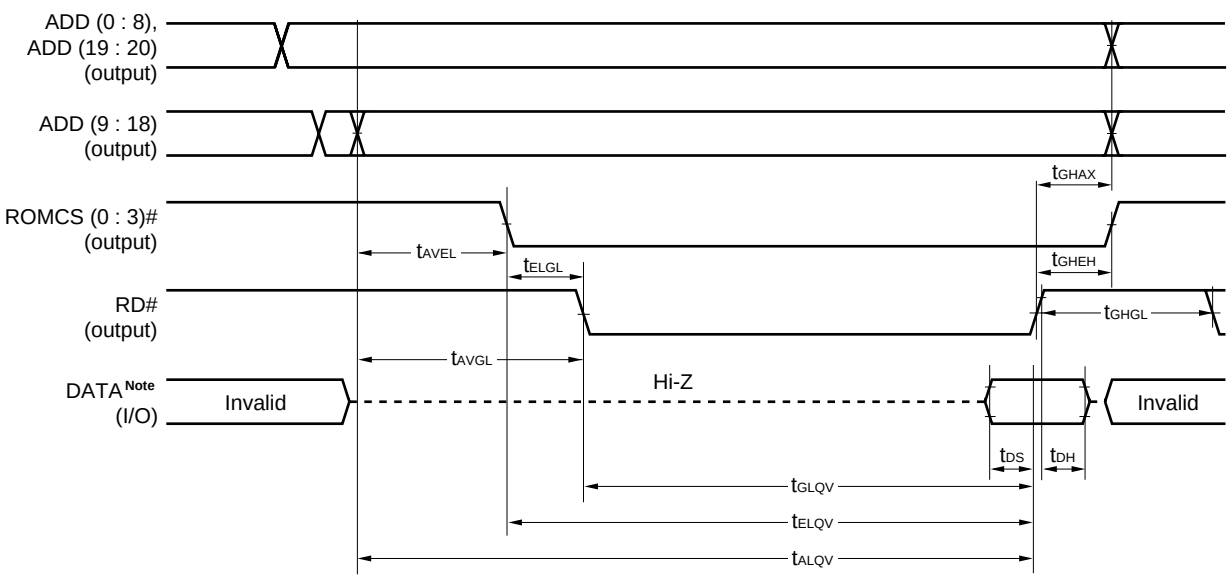
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Write cycle time	t_{AVAV}		150		ns
Address setup time (to WR# ↑)	t_{AVWH}		75		ns
Address setup time (to ROMCS (0:3)# ↓)	t_{AVEL}		0		ns
ROMCS (0:3)# setup time (to WR# ↓)	t_{ELWL}		10		ns
WR# pulse width	t_{WLWH}		75		ns
ROMCS (0:3)# hold time (from WR# ↑)	t_{WHEH}		10		ns
Address hold time (from WR# ↑)	t_{WHAX}		10		ns
WR# high-level width	t_{WHWL}		75		ns
Address setup time (to WR# ↓)	t_{AVWL}		25		ns
Data setup time (to WR# ↑)	t_{DVWH}		75		ns
Data hold time (from WR# ↑)	t_{WHDX}		10		ns



Note In 32-bit mode: DATA (16:31)/GPIO (16:31) or DATA (0:15)
In 16-bit mode: DATA (0:15)

(9) Flash memory mode read parameter

Parameter	Symbol	MIN.	MAX.	Unit
Data output delay time from address (ADD (0:25))	t_{AVQV}	180		ns
Data output delay time from ROMCS (0:3)#	t_{ELQV}	180		ns
Address (ADD (0:25)) setup time (to ROMCS (0:3)# ↓)	t_{AVEL}	0		ns
Data output delay time from RD#	t_{GLQV}	80		ns
Address (ADD (0:25)) setup time (to RD# ↓)	t_{AVGL}	0		ns
ROMCS (0:3)# hold time (from RD# ↑)	t_{GHEH}	10		ns
Address (ADD (0:25)) hold time (from RD# ↑)	t_{GHAX}	10		ns
RD# high-level width	t_{GHGL}	75		ns
Data input setup time	t_{DS}	0		ns
Data input hold time	t_{DH}	6		ns
ROMCS (0:3)# setup time (to RD#)	t_{ELGL}	10		ns



Note In 32-bit mode: DATA (16:31)/GPIO (16:31) or DATA (0:15)
In 16-bit mode: DATA (0:15)

(10) System bus parameter (IOCHRDY) (1/2)

Parameter	Symbol	MIN.	MAX.	Unit
BUSCLK low-level pulse width	t_{BCLKL}	45		ns
BUSCLK high-level pulse width	t_{BCLKH}	45		ns
Address (ADD (0:25)) setup time (to BUSCLK ↓)	t_{AVCK}	15		ns
Address (ADD (0:25)) setup time (to command signal ↓)Notes 1, 2	t_{AVCL}	T × N – 29		ns
Address hold time (from command signal ↑)Note 1	t_{CHAV}	25		ns
Command signal setup time (to BUSCLK ↑)Note 1	t_{CLCK}	15		ns
Command signal low-level widthNote 1, 2	t_{CLCH}	2 × T × N – 29		ns
Command signal recovery timeNote 1	t_{CHCL}	T × (N + 1) – 29		ns
IOCHRDY sampling time	t_{CLR}	0	T × N – 44	ns
Command signal low-level width from ready signalNotes 1, 2	t_{RHCH}	T × N	2 × T × N + 29	ns
IOCHRDY hold time (from command signal ↑)Note 1	t_{CHRL}	0		ns
Data output setup time (to command signal ↓)Note 1	t_{DVCL}	0		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}	25		ns
Data input setup time (to command signal ↑)	t_{DS}	0		ns
Data input hold time (from command signal ↑)	t_{DH}	15		ns

Notes 1. With the VR4102, the MEMW#, MEMR#, IOW#, and IOR# pins are called the command signals for the system bus interface.

2. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD#/CLKSEL2, RTS#CLKSEL1, and DTR#CLKSEL0).

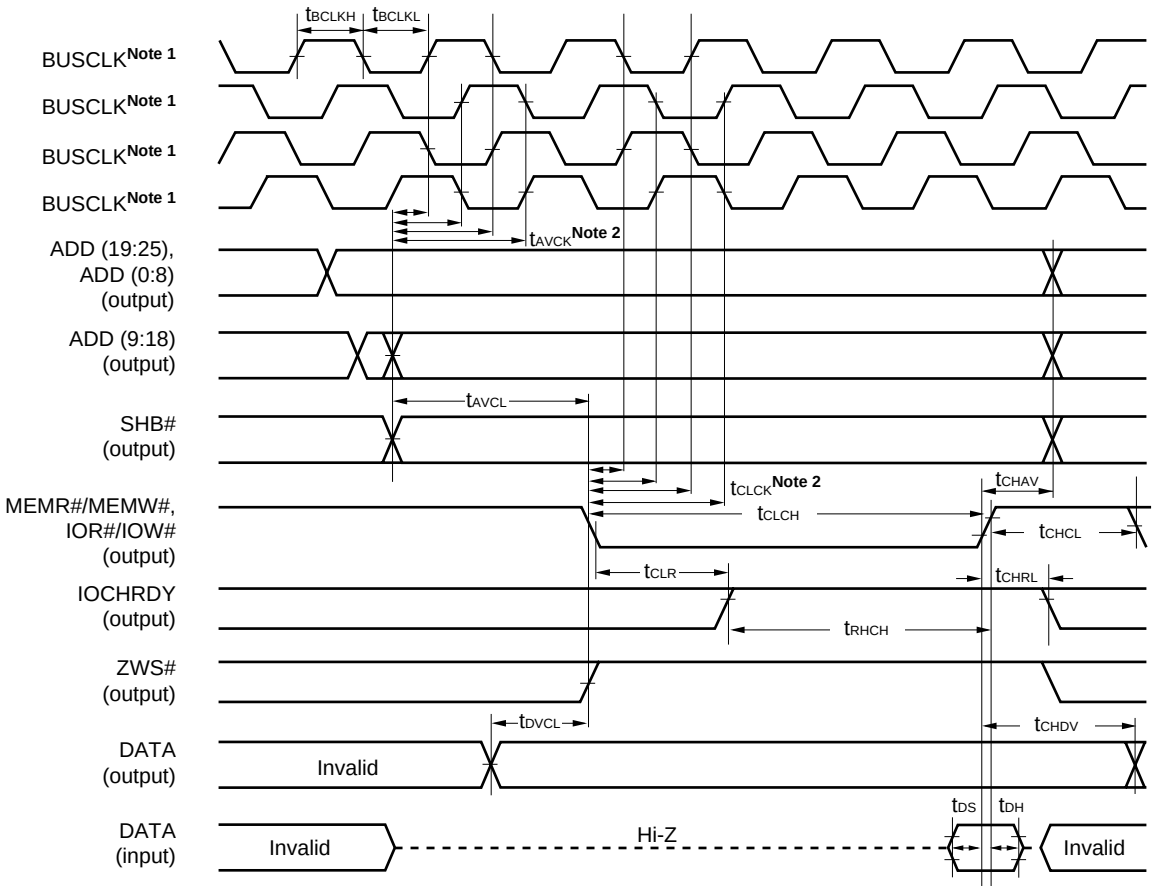
CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1	0	1	37.3
1	0	0	40.6

WISAA2	WISAA1	WISAA0	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1Note	0Note	0Note	4
1Note	0Note	1Note	3
1	1	0	—
1	1	1	—

Note If the WISAA (0:2) bits are set to 100B or high, the AC characteristics of t_{AVCK} and t_{CLCK} are not guaranteed.

(10) System bus parameter (IOCHRDY) (2/2)

When WISAA (0:2) = 010B



Notes 1. BUSCLK indicates that there are four possible relationships between BUSCLK and other system bus interface signals.

2. This indicates the minimum setup time to the BUSCLK rising or falling edge.

(11) System bus parameter (ZWS#) (1/2)

Parameter	Symbol	MIN.	MAX.	Unit
Command signal low-level width[Notes 1, 2]	t_{CLCH}	T × N – 31		ns
ZWS# delay time (from command signal)[Notes 1, 2]	t_{CLZL}		T × (N – 1) – 20	ns
ZWS# hold time (from command signal)[Note 2]	t_{CHZH}	0		ns

Notes 1. With the VR4102, the MEMW#, MEMR#, IOW#, and IOR# pins are called the command signals for the system bus interface.

2. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD#/CLKSEL2, RTS#CLKSEL1, and DTR#CLKSEL0).

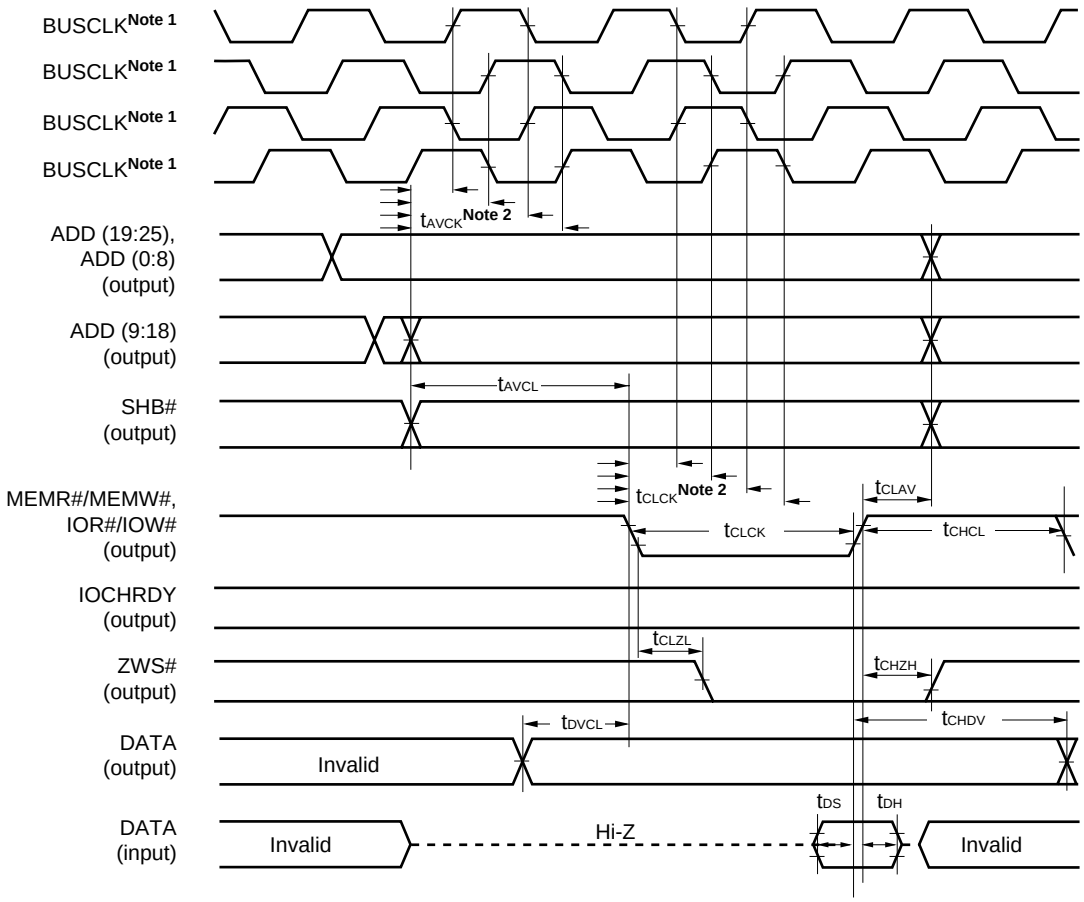
CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1	0	1	37.3
1	0	0	40.6

WISAA2	WISAA1	WISAA0	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1[Note]	0[Note]	0[Note]	4
1[Note]	0[Note]	1[Note]	3
1	1	0	—
1	1	1	—

Note If the WISAA (0:2) bits are set to 100B or high, the AC characteristics of t_{AVCK} and t_{CLCK} are not guaranteed.

(11) System bus parameter (ZWS#) (2/2)

When WISAA (0:2) = 101B



Notes 1. BUSCLK indicates that there are four possible relationships between BUSCLK and other system bus interface signals.

2. This indicates the minimum setup time to the BUSCLK rising or falling edge.

(12) High-speed system bus parameter (IOCHRDY) (1/2)

Parameter	Symbol	MIN.	MAX.	Unit
Address (ADD (0:25)) setup time (to command signal ↓)**Notes 1, 2**	t_{AVCL}	T × N – 29		ns
Command signal low-level width**Notes 1, 2**	t_{CLCH}	T × (N + M) – 29		ns
Address hold time (from command signal ↑)**Note 1**	t_{CHAV}	25		ns
Command signal recovery time**Note 1**	t_{CHCL}	T × (N + 1) – 29		ns
IOCHRDY sampling start time	t_{CLR}	0		ns
Command signal output hold time (from IOCHRDY ↑)**Notes 1, 2**	t_{RHCH}	T × M	T × (N + M) + 29	ns
IOCHRDY hold time (from command signal ↑)**Note 1**	t_{CHRL}	0		ns
Data output setup time (to command signal ↓)**Note 1**	t_{DVCL}	–15		ns
Data output hold time (from command signal ↑)**Note 1**	t_{CHDV}	25		ns
Data input setup time (to command signal ↑)**Note 1**	t_{DS}	0		ns
Data input hold time (from command signal ↑)**Note 1**	t_{DH}	15		ns

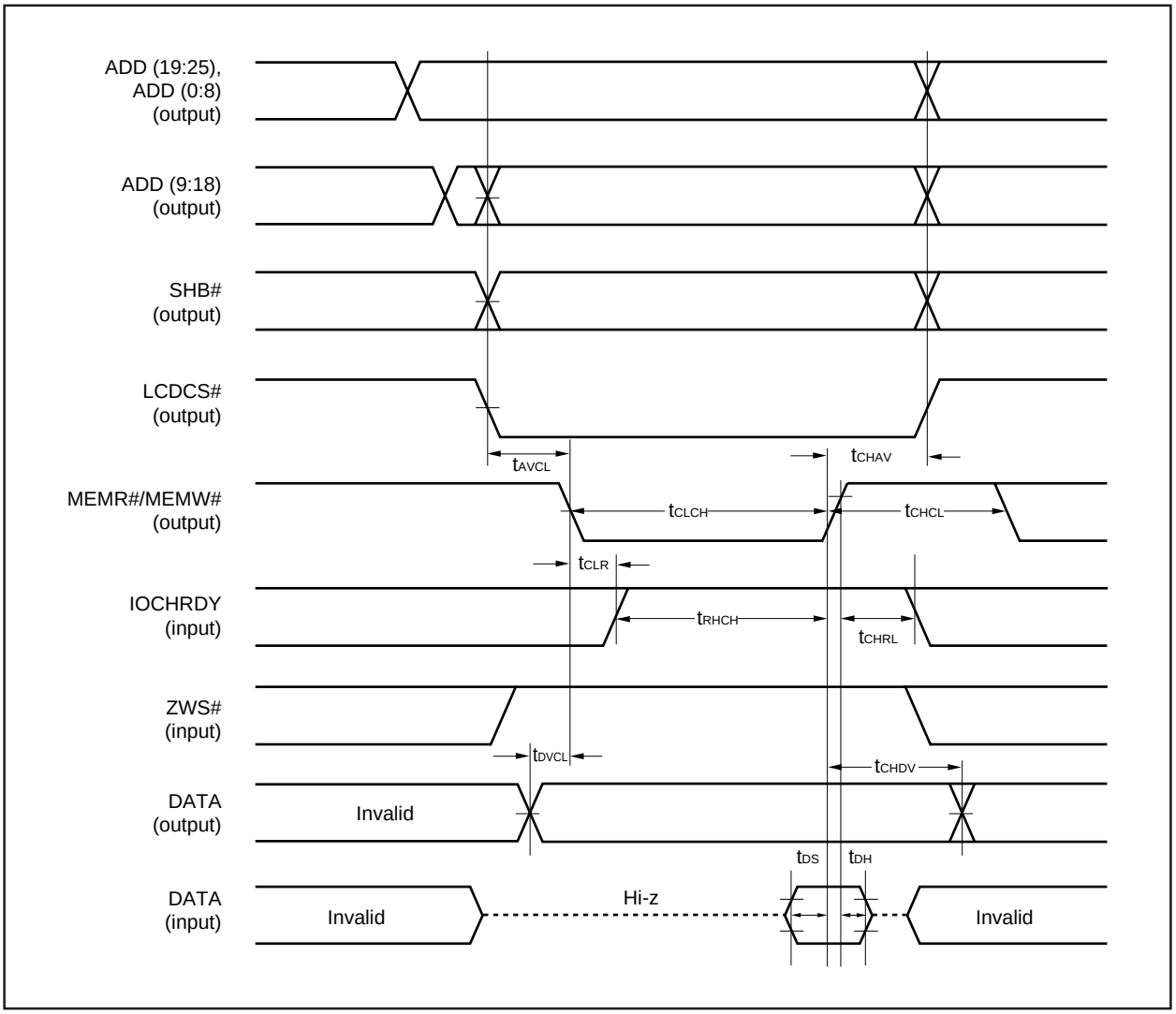
Notes 1. With the VR4102, the MEMR# and MEMW# signals are called the command signals for the high-speed system bus interface.

2. The values of N and M are set by using the WLCD/M (0:2) bits of the BCUSPEEDREG register. The value of T is set by using the CLKSEL (0:2) bits (TxD#/CLKSEL2, RTS#CLKSEL1, and DTR#CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1	1	0	33.8
1	0	1	37.3

WLCD/M2	WLCD/M1	WLCD/M0	N (TClock)	M (TClock)
0	0	0	8	8
0	0	1	7	7
0	1	0	6	6
0	1	1	5	5
1	0	0	4	4
1	0	1	3	3
1	1	0	2	2
1	1	1	1	2

(12) High-speed system bus parameter (IOCHRDY) (2/2)



(13) High-speed system bus parameter (ZWS#) (1/2)

Parameter	Symbol	MIN.	MAX.	Unit
Command signal low-level width[Notes 1, 2]	t_{CLCH}	T × N – 31		ns
ZWS# signal delay time (from command signal ↑)[Notes 1, 2]	t_{CLZL}		T × (N – 1) – 20	ns
ZWS# signal hold time (from command signal ↑)[Note 1]	t_{CHZH}	0		ns

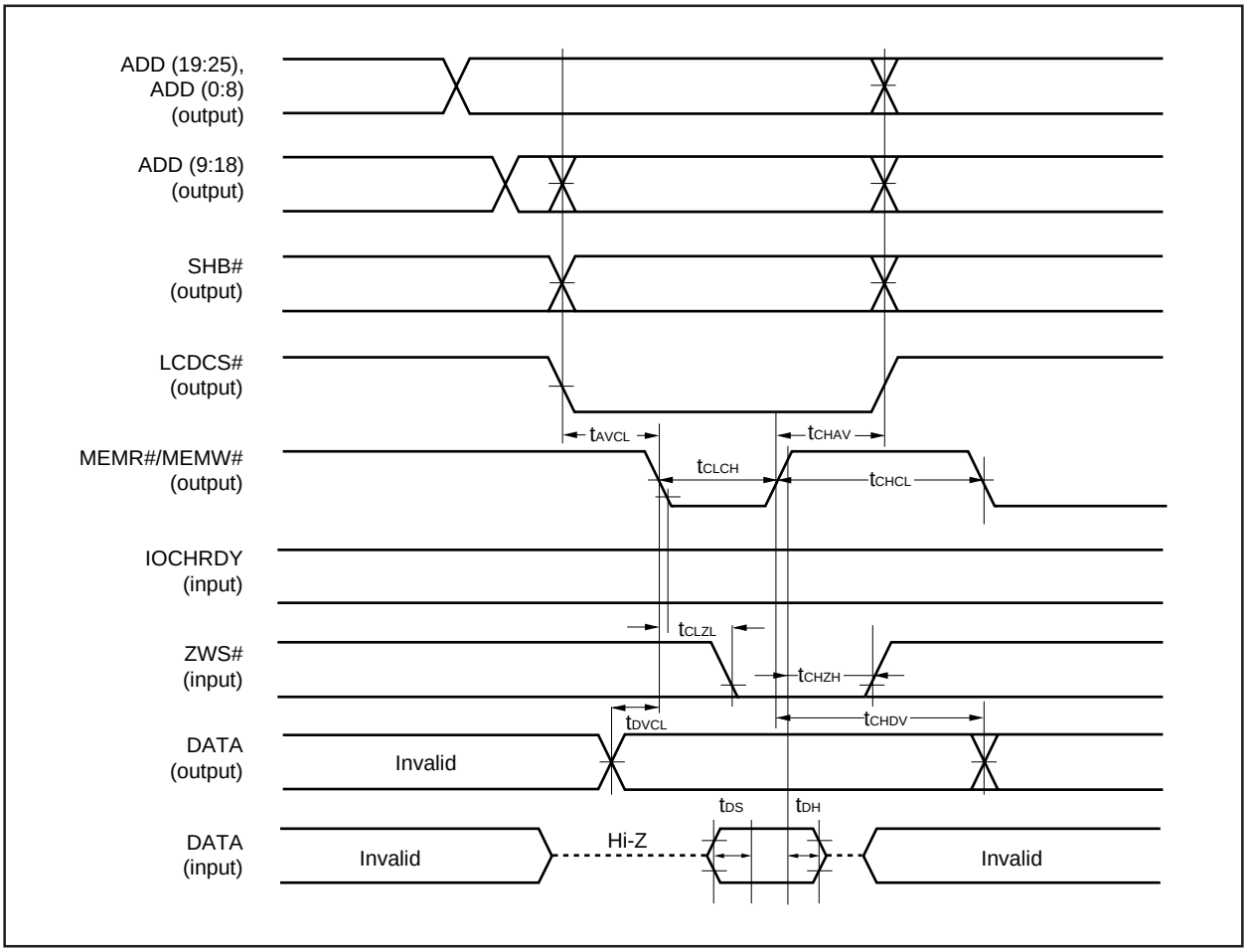
Notes 1. With the VR4102, the MEMR#, MEMW#, IOW#, and IOR# signals are called the command signals for the system bus interface.

2. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD#/CLKSEL2, RTS#CLKSEL1, and DTR#CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1	0	1	37.3
1	0	0	40.6

WISAA2	WISAA1	WISAA0	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	2
1	1	1	1

(13) High-speed system bus parameter (ZWS#) (2/2)



(14) LCD interface parameter

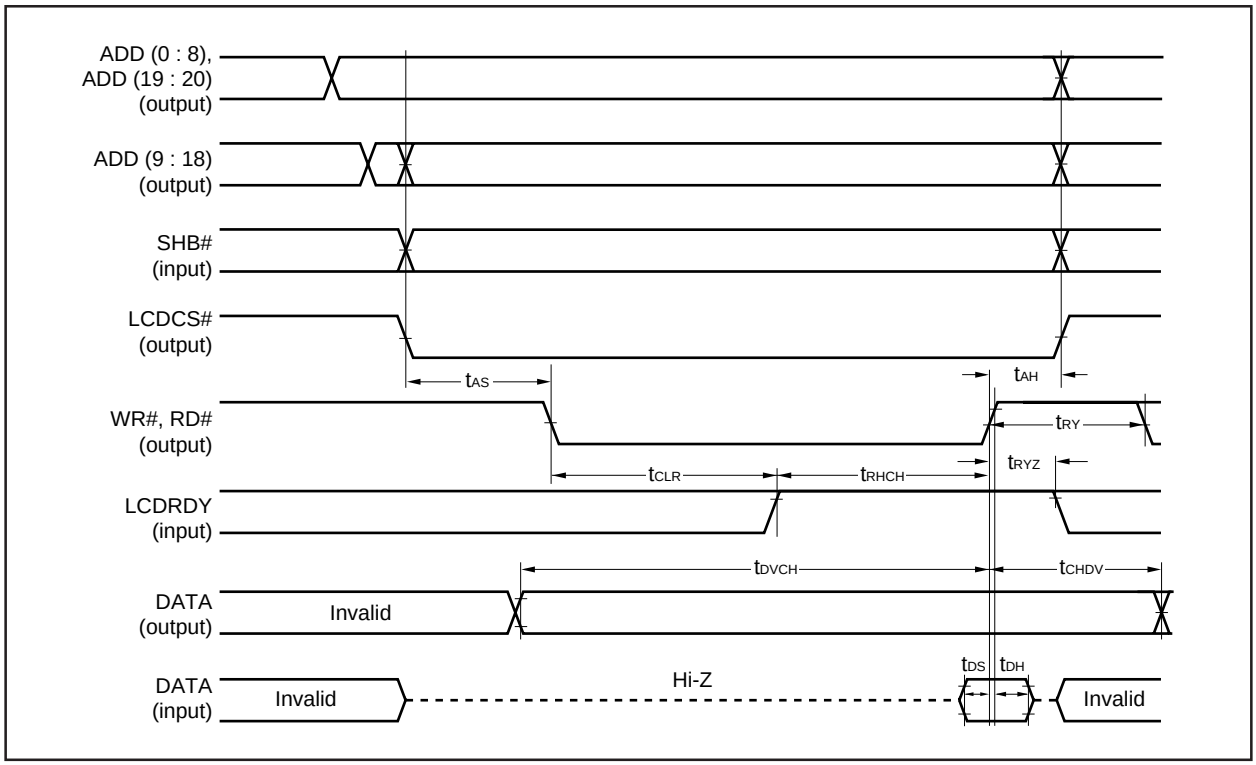
Parameter	Symbol	MIN.	MAX.	Unit
Address setup time (to command signal ↓)Note 1	t_{AS}	15		ns
Address hold time (from command signal ↑)Note 1	t_{AH}	0		ns
Command signal recovery timeNote 1	t_{RY}	30		ns
LCDRDY sampling time	t_{CLR}	0		ns
Command signal output hold time (from LCDRDY ↑)Notes 1, 2	t_{RHCH}	T × N	T × (N + 2) + 29	ns
LCDRDY hold time (from command signal ↑)Note 1	t_{RYZ}	0		ns
Data output setup time (to command signal ↑)Notes 1, 2	t_{DVCH}	T × (N + 2)		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}	25		ns
Data input setup time (to command signal ↑)Note 1	t_{DS}	0		ns
Data input hold time (from command signal ↑)Note 1	t_{DH}	15		ns

Notes 1. With the V_R4102, the RD# and WR# signals are called the command signals for the LCD interface.

2. The value of N is set by using the WLCD/M (0:1) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD#/CLKSEL2, RTS#CLKSEL1, and DTR#CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1	0	1	37.3
1	0	0	40.6

WLCD/M1	WLCD/M0	N (TClock)
0	0	8
0	1	6
1	0	4
1	1	2



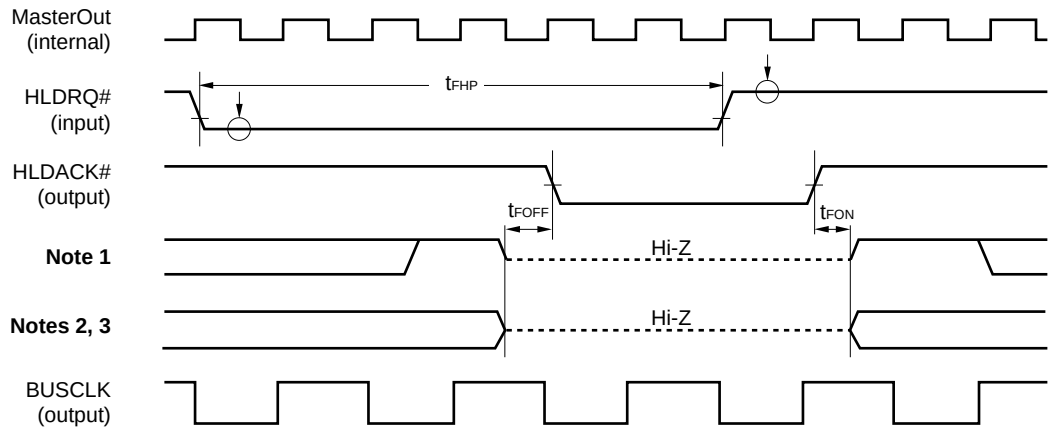
(15) Bus hold parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
HLDRQ# input pulse width[Note]	t_{FHP}	In Full-speed/standby mode	3T		ns
Data floating delay time	t_{FOFF}	In Full-speed/standby mode	0		ns
Data valid delay time	t_{FON}	In Full-speed/standby mode	0		ns
HLDRQ# input pulse width[Note]	t_{SHP}	In Suspend mode	6T		ns
Data floating delay time	t_{SOFF}	In Suspend mode	0		ns
Data valid delay time	t_{SON}	In Suspend mode	0		ns
MRAS (0:3)# precharge time	t_{RPS}	In Suspend mode	110		ns
UCAS#/LCAS# setup time	t_{CSR}	In Suspend mode	5		ns

Note The value of T is set by using the CLKSEL (0:2) bits (TxD#/CLKSEL2, RTS#CLKSEL1, and DTR#CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1	0	1	37.3
1	0	0	40.6

(a) Bus hold in Full-speed/Standby mode

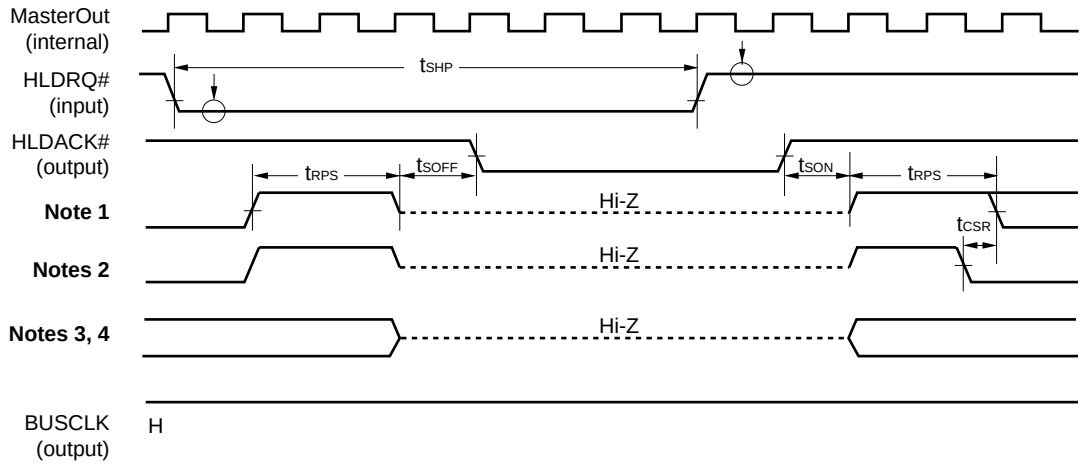


Notes 1. UUCAS#/MRAS3#, ULCAS#/MRAS2#, MRAS (0:1)#, UCAS#, LCAS#

2. SHB#, IOR#, IOW#, MEMR#, MEMW#, RD#, WR#, ADD (0:25), DATA (0:15)

3. In 32-bit data bus mode: DATA (16:31)/GPIO (16:31)

(b) Bus hold in Suspend mode



Notes 1. In 32-bit mode: MRAS (0:1)#
In 16-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, MRAS (0:1)#

2. In 32-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, UCAS#, LCAS#
In 16-bit mode: UCAS#, LCAS#

3. SHB#, IOR#, IOW#, MEMR#, MEMW#, RD#, WR#, ADD (0:25), DATA (0:15)

4. In 32-bit data bus mode: DATA (16:31)/GPIO (16:31)

(16) Keyboard Interface parameter

Parameter	Symbol	MIN.	MAX.	Unit
High-level width[Note 1]	t_{SCAN}	30K – 1	30.16K + 1	μs
Idle time (KSCANn ↓ → KSCAN (n+1) ↑)[Note 2]	t_{KWAIT}	30L – 1	30.16L + 1	μs
Key scan interval time[Note 3]	t_{KI}	30M – 1	30.16M + 1	μs
Key input setup time (to KSCANn ↑)[Note 4]	t_{KS}	30N – 1		μs
Key input hold time (from KSCANn ↑)	t_{KH}	0		μs

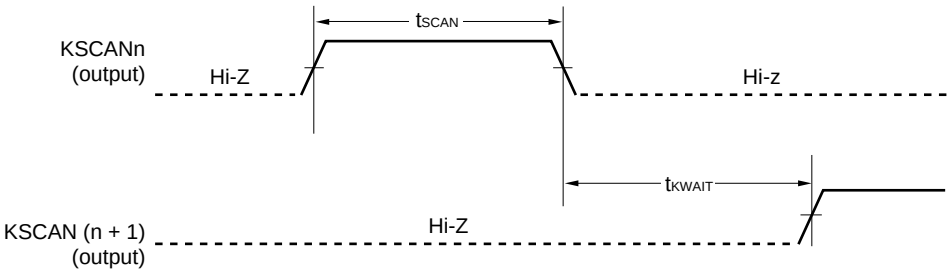
Notes 1. K: Sum of the values set to the T1CNT (0:4) bits and T2CNT (0:4) bits of the KIUWKSREG register

2. L: Value set to the T3CNT (0:4) bits of the KIUWKSREG register

3. M: Value set to KIUWKIREG register

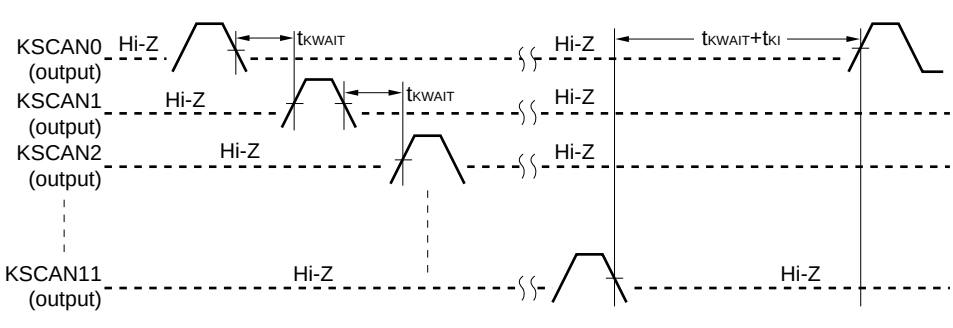
4. N: Value set to the T1CNT (0:4) bits of the KIUWKSREG register

(a) Keyboard scan parameter 1

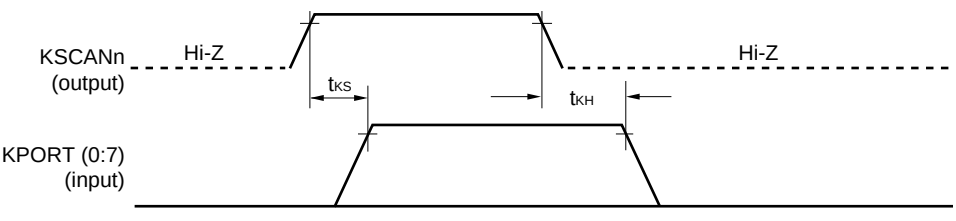


Remark n = 0 to 7

(b) Keyboard scan parameter 2



(c) Keyboard parameter 3



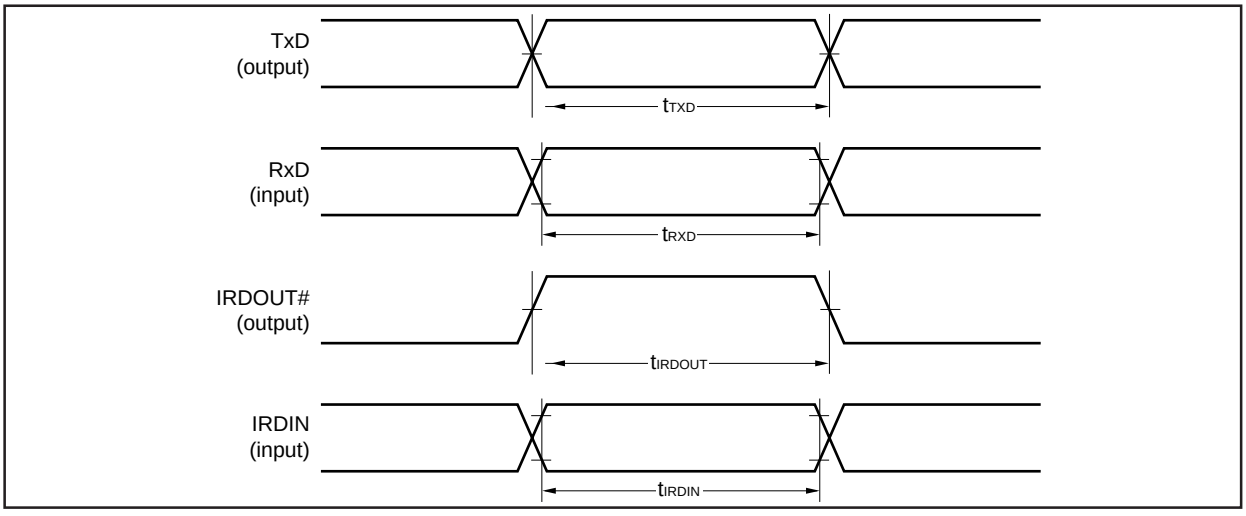
Remark n = 0 to 7

(17) Serial interface parameter

Parameter	Symbol	MIN.	MAX.	Unit
TxD output pulse width[Note]	t_{TXD}	N – 1	N + 1	μs
RxD input pulse width[Note]	t_{RXD}	(9/16)N		μs
IRDOUT high-level output pulse width[Note]	t_{IRDOUT}	(3/16)N – 1	(3/16)N + 1	μs
IRDIN input pulse width	t_{IRDIN}	1		μs

Note N: Data transfer rate per bit, which is determined by the divisor of the baud-rate generator that is set with the SIUDLL and SIUDLM registers.

Baud Rate (bps)	SIUDLM, SIUDLL	N (μs)
50	23040	20000
75	15360	13333
110	10473	9091
134.5	8565	7435
150	7680	6667
300	3840	3333
600	1920	1667
1200	920	833
1800	640	556
2000	573	500
2400	480	417
3600	320	278
4800	240	208
7200	160	139
9600	120	104
19200	60	52.1
38400	30	26.0
56000	21	17.9
128000	9	7.81
144000	8	6.94
192000	6	5.21
230400	5	4.34
288000	4	3.47
384000	3	2.60
576000	2	1.74
1152000	1	0.868

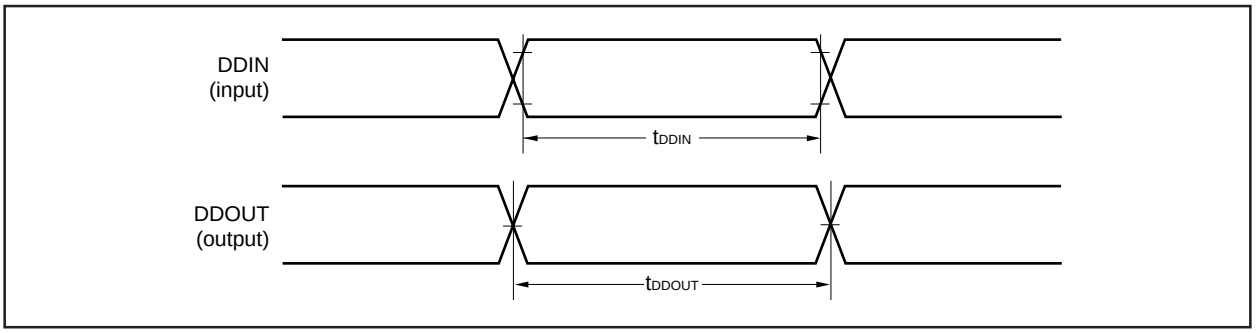


(18) Debug serial interface parameter

Parameter	Symbol	MIN.	MAX.	Unit
DDOUT output pulse width[Note]	t_{DDOUT}	N – 1	N + 1	μs
DDIN input pulse width[Note]	t_{DDIN}	(9/16)N		μs

Note N: Transfer rate of baud rate per bit set to the BPR0 (0:2) bits of the BPRM0REG register

BPRM0REG	Baud Rate (bps)	N (μs)
111	115200	8.68
110	57600	17.36
101	38400	26.04
100	19200	52.03
011	9600	104.16
010	4800	208.33
001	2400	416.66
000	1200	833.33



(19) HSP interface parameter

Parameter	Symbol	MIN.	MAX.	Unit
SDO output delay time[Note 1]	t_{SDOD}		15	ns
SDI setup time[Note 2]	t_{SDIS}	25		ns
SDI hold time[Note 2]	t_{SDIH}	0		ns
FS setup time[Note 2]	t_{FSIS}	20		ns
FS hold time[Note 2]	t_{FSIH}	0		ns

Notes 1. The reference clock of this parameter is the rising edge of HSPSCLK.

2. The reference clock of this parameter is the falling edge of HSPSCLK.

LOAD COEFFICIENT (DELAY TIME PER LOAD CAPACITANCE)

Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			5	ns/20 pF

A/D converter characteristics (T_A = –10 to +70°C, V_{DD} = +3.0 to 3.6 V)

Parameter	Symbol	MIN.	MAX.	Unit
Resolution		10		bit
Zero-scale error[Notes 1, 2]	ZSE	0	±4.0	LSB
Full-scale error[Notes 1, 2]	RSE	0	±5.0	LSB
Integral linearity error[Notes 1, 2]	INL	0	±3.0	LSB
Differential linearity error[Notes 1, 2]	DNL	0	±3.0	LSB
Analog input voltage[Notes 1, 3]	VIAN	–0.3	AV_{DD} + 0.3	V

Notes 1. Applied to TPX (0:1), TPY (0:1), ADIN (0:2), and AUDIOIN pins.

2. Quantization error is excluded.

3. AV_{DD} is the dedicated V_{DD} for the A/D converter.

D/A converter characteristics (T_A = –10 to +70°C, V_{DD} = +3.0 to 3.6 V)

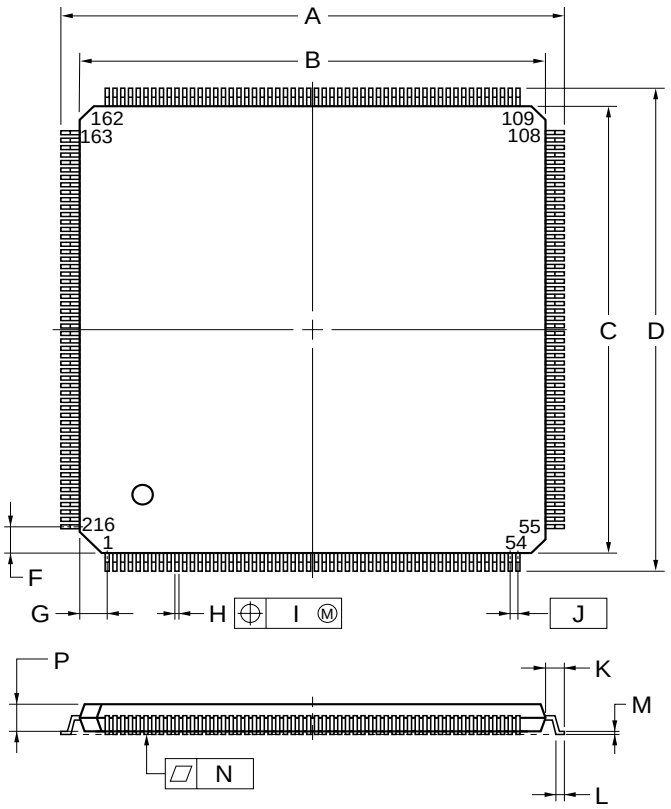
Parameter	Symbol	MIN.	MAX.	Unit
Resolution		10		bit
Integral linearity error[Notes 1, 2]	INL	0	±3.0	LSB
Differential linearity error[Notes 1, 2]	DNL	0	±3.0	LSB

Notes 1. Applied to AUDIOOUT pin.

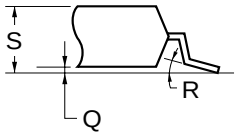
2. Quantization error is excluded.

24. PACKAGE DRAWINGS

216 PIN PLASTIC LQFP (FINE PITCH) (24x24)



detail of lead end



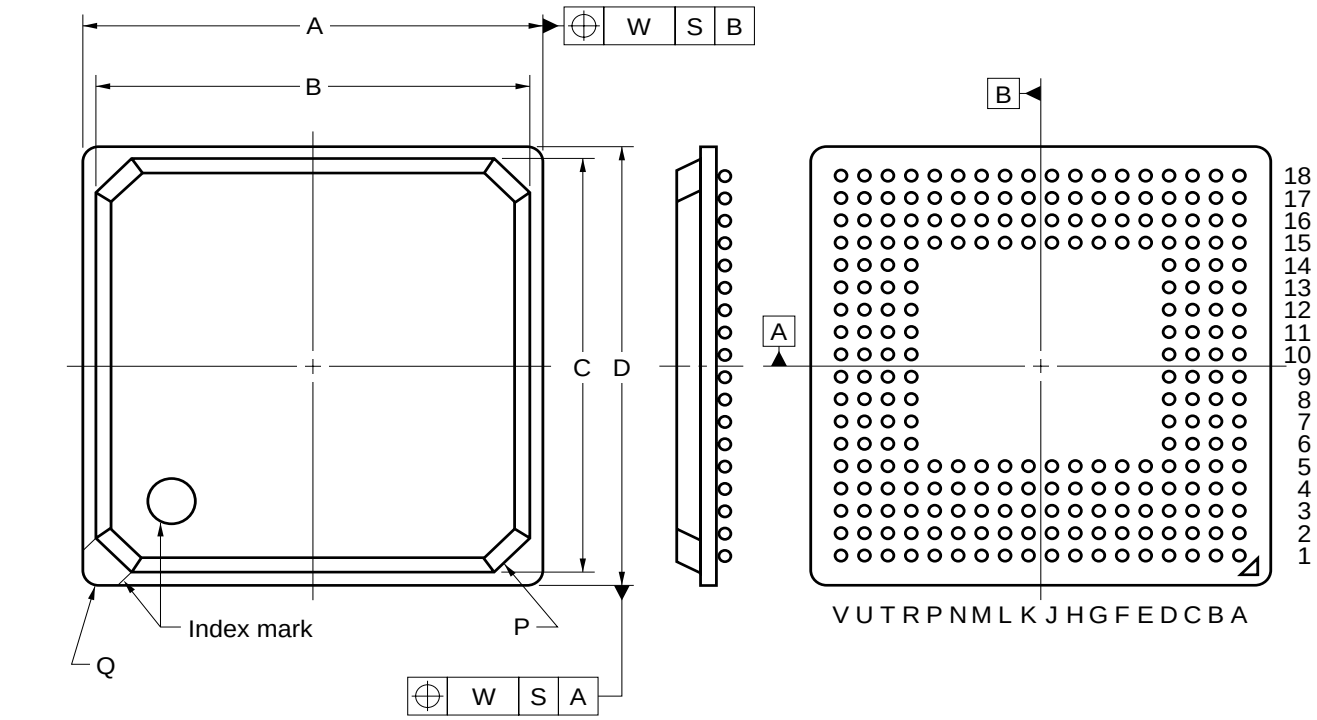
NOTE

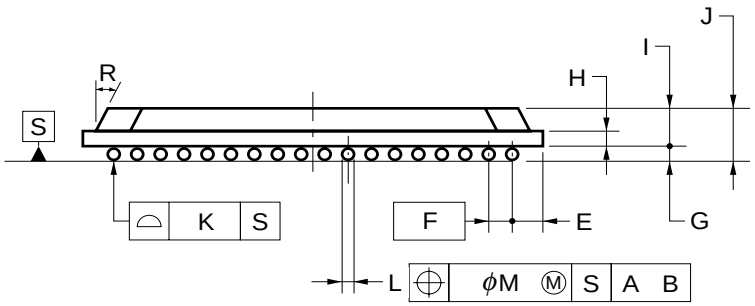
Each lead centerline is located within 0.07 mm (0.003 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	26.00±0.20	$1.024^{+0.008}_{-0.009}$
B	24.00±0.20	0.945±0.008
C	24.00±0.20	0.945±0.008
D	26.00±0.20	$1.024^{+0.008}_{-0.009}$
F	1.40	0.055
G	1.40	0.055
H	0.18±0.05	0.007±0.002
I	0.07	0.003
J	0.40 (T.P.)	0.016 (T.P.)
K	1.00±0.20	$0.039^{+0.009}_{-0.008}$
L	0.50±0.20	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.08	0.003
P	$1.40^{+0.10}_{-0.05}$	$0.055^{+0.004}_{-0.002}$
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.	0.067 MAX.

S216GM-40-8EV

★ 224 PIN FINE PITCH BGA (16x16)





ITEM	MILLIMETERS	INCHES
A	16.00±0.10	0.630±0.004
B	15.4	0.606
C	15.4	0.606
D	16.00±0.10	0.630±0.004
E	1.20	0.047
F	0.8 (T.P.)	0.031 (T.P.)
G	0.35±0.1	$0.014^{+0.004}_{-0.005}$
H	0.36	0.014
I	0.96	0.038
J	1.31±0.15	$0.052^{+0.006}_{-0.007}$
K	0.10	0.004
L	$0.50^{+0.05}_{-0.10}$	$0.020^{+0.002}_{-0.004}$
M	0.08	0.003
P	C1.0	C0.039
Q	R0.3	R0.012
R	25°	25°
W	0.20	0.008

S224S1-3C

NOTES

1. Controlling dimension —— millimeter.

2. Each ball centerline is located within φ0.08 mm (φ0.003 inch) of its true position (T.P.) at maximum material condition.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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J97. 8

Related documents VR4100 User's Manual (U10050E)
VR4102 User's Manual (U12739E)
VR4111 User's Manual (Under preparation)

Reference document Glossary of Technical Terms (IEI-601)[Note]

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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