This sections covers the Performance registers of the Coherency Manager

CM Performance Registers - Offset 0x6000

Name	Offset	Description	Type
Counter Control Register	0x100	Controls starting/stopping of Performance Counters.	R/W
Counter Overflow Status	0x120	Indicates which performance counters have overflowed	R/W
Counter Event Select	0x130	Selects event type of each performance counter	R/W
Performance Cycle Counter	0x180	CM Cycle count value.	R/W
Counter 0 Qualifier	0x190	Performance counter 0 event qualifiers.	R/W
Performance Counter 0	0x198	Performance Counter 0 value.	R/W
Counter 1 Qualifier	0x1a0	Performance counter 1 event qualifiers	R/W
Performance Counter 1	0x1a8	Performance Counter 1 value	R/W

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Within the Global Debug Block is a set of registers you can use to get CM Performance information. These registers are offset hex 6000 from the starting address of the GCR.

Here's an overview of the CM Performance registers and their offsets. I'll go into each register's details in subsequent slides.

Performance characteristics of the CM can be measured via the 3 CM performance counters. There are two identical 32-bit performance counters that can be programmed to count CM specific events and there is an additional 32-bit cycle counter register.

The counters are started and reset by using bits in the Performance Counter Control Register. There are also bits in the Performance Counter Control Register that determine what to do on counter overflow.

When a performance counter overflows, the corresponding bit is automatically set in the CM Performance Counter

Overflow Status Register. The overflow status bit is cleared by writing a 1 to it in this register.

The event to be counted by each performance counter is designated by the event number set in the Event Select 0 and

1 fields of the CM Performance Counter Event Selection Register.

Each event is further specified by a corresponding CM Performance Counter Qualifier Register.

CM Performance Counter Control Register

Register Fields		CM Performance Counter Control Register (GCR_DB_PC_CTL Offset 0x0100)	Reset State
Name	Bits		
Perf_Int_En	30	Enable Interrupt on counter overflow	0
Perf_Ovf_Stop	29	Stop Counting on overflow.	0
P1_Reset	9	Counter 1 and P1_Overflow bit is reset before counting is started.	0
P1_CountOn	8	Start Counting Counter 1	0
P0_Reset	7	Counter 0 and P0_Overflow bit is reset before counting is started.	0
P0_CountOn	6	Start Counting Counter 0	0
Cycl_Cnt_Reset	5	Cycle Counter and its overflow bit is reset before counting is started.	0
Cycl_Cnt_CountOn	4	Start Cycle Counter	0
Perf_Num_Cnt	3-0	The number of performance counters implemented (not including the cycle counter).	2

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With the CM performance counter control register you can configure the behavior of the performance counters.

If the Performance interrupt enable bit is set, an interrupt is generated when any counter, including the cycle counter reaches its maximum value of 0xFFFFFFFF. Note: The CM asserts the Coherency Manager Program Counter Interrupt signal, CM_PCInt which generates an interrupt only if the System Integrator has connected CM_PCInt to one bit, SI_CMInt, of the System Interface Coherency Manager Interrupt Block.

If the performance overflow stop bit, Perf_Ovf_Stop , is set to 1, then all CM Performance counters will stop counting when any counter, including the Cycle Counter, reaches its maximum value of 0xFFFFFFFF. If it is not set then when a counter overflows, it rolls over and continues counting from 0.

Setting Performance 1 Reset, Performance 0 Reset or Cycle Count Reset resets the corresponding performance counter register along with its corresponding overflow bit in the counter overflow status register prior to the start of counting.

Setting Performance 1 Count On, Performance 0 Count On or Cycle Count On Starts the counting of the corresponding counter.

Reset bits and start bits can be set in the same access. This functionality allows all three counters to be reset and started with a single GCR write.

The Performance Number Count tells you the number of performance counters you have in the system. This will always be set to 2.

CM Performance Counter Overflow Status Register Offset 0x120

Register Fields		CM Performance Counter Overflow Status Register (GCR_DB_PC_OV Offset 0x120)	Reset State
Name	Bits		
P1_Overflow	2	If this bit is set to 1, CM Performance Counter 1 has overflowed	0
P0_Overflow	1	If this bit is set to 1, CM Performance Counter 0 has overflowed	0
Cycl_Cnt_Overflow	0	If this bit is set to 1, the CM Cycle Counter Register has Overflowed.	0

When a performance counter overflows, the corresponding bit is automatically set in the CM Performance Counter

Overflow Status Register. A status bit is cleared by writing a 1 to it.

CM Performance Counter Event Select Register

Register Fields		CM Performance Counter Event Select Register (GCR_DB_PC_EVENT Offset 0x130)	Reset State
Name	Bits		
P1_Event	15 - 8	Event Selection for CM Performance Counter 1	0
P0_Event	7 - 0	Event Selection for CM Performance Counter 0	0

0	Request Count	Measures System load
1	Coherent Request or Response	Count specified request/response type
2	CM Write Data Usage	L2 to Memory Write Data cycles
3	CM Command Bus Usage	L2 to Memory command cycles
4	CM Read Data Usage	L2 to Memory Read Data Cycles
5	Sharing Miss	Counts Read from Specific CPU
6	Response Unit Usage	CPU to IOCU read bus load
8	* L2 Pipeline Utilization	Counts starts into the TA stage of the L2
9	* L2 Hits/Misses	Counts different types of L2 Cache Hits and Misses, crossed with Source Port ID.
16	1st IOCU Requests	Requests received by 1st IOCU
17	* 2nd IOCU Requests	Requests received by 2nd IOCU

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The event select register is divided into 2 parts for counter 0 and 1. There are 10 events that can be counted. Each of these events is further qualified by settings in the counter qualifier registers.

Event 0 is the request count. It can be qualified by CPU or IOCU ports, cache coherency attributes, command requests, request length and request target. It would be useful to use the request count along with the cycle count to get an idea of requests received over a period of time.

Event 1 counts Requests and responses to requests that can be qualified by intervention states, speculative or no-speculative Coherent Read requests and intervention Command requests from a load or a store that missed in the L1 cache.

Event 2 counts the write Data bus Usage which is the number of cycles the L2-Memory write data bus is in use. This event can be qualified to count stall cycles or not.

Event 3 counts Command bus usage which is the number of cycles the command data bus is in use. This event can also be qualified to count stall cycles or not.

Event 4 counts Read Data bus Usage which is the number of cycles the L2-Memory read data bus is in use. This event can also be qualified to count stall cycles or not.

Event 5 counts Sharing Miss which is the number of cache misses that were satisfied by another processor. This event can be qualified by specifying which CPUs should participate in the count.

Event 6 counts Response Unit Usage which is the number of d-words on the processor IOCU read data bus for a specific CPU.

Event 8 counts L2 pipe line usage Qualified by a start that was stalled, requested started an not stalled, waiting for sync to clear, request stalled, request denied or request started.

Event 9 counts L2 hit/misses see Software Users manual for more information.

Event 16 and 17 count IOCU requests - different requests received by the IOCU that can be qualified with a transaction ID, I/O Parking state, Number of transactions in a request, Burst length, L2 Allocation type, Posted or non-posted writes, Cacheability, and by read or write requests.

For more information see the Software Users Manual section "CM Performance Counter Event Types and Qualifiers"

CM Performance Counter Qualifier Registers

- Counter 0 Qualifier GCR Offset 0x190
- Counter 1 Qualifier GCR Offset 0x1a0

Register Fields		CM Performance Counter Qualifier Field Register (GCR_DB_PC_QUAL Offset 0x190, 0x1a0)	Reset State
Name	Bits		
P0/1_Qualifier	31 - 0	CM Performance Counter Event Qualifier. The qualifier corresponds to the event configured through the Performance Counter Event Select Register.	0

These are the qualifier registers, one for each counter. These are used to configure the qualifiers for the events discussed in the last slide.
The qualifiers for some events are composed of several groups. A performance counter will increment if the specified event occurs and the qualifier criteria is matched in all groups.

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These are the qualifier registers, one for each counter. These are used to configure the qualifiers for the events I discussed in the last slide.

The qualifiers for some events are composed of several groups. A performance counter will increment if the specified

event occurs and the qualifier criteria is matched in all groups.

You should refer to the Coherent Processing System User's manual for your core for the specific qualifier values for each event.

CM Counter Registers

Register Fields		CM Cycle Counter Register (GCR_DB_PC_CYCLE Offset 0x180)	Reset State
Name	Bits		
Cycl_Cnt	31 - 0	32-bit count of CM clock cycles.	0

Register Fields		CM Performance Counter n Register (GCR_DB_PC_CNTn Offset 0x198,0x1a8)	Reset State
Name	Bits		
Pn_Count	31:0	32-bit Performance Counter. The event counted is specified in the CM Performance Counter Event Select Register and by the corresponding Qualifier Register.	0

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Here are the 3 counters and their offsets.