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Cluster Power Controller (CPC)
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Cluster Power Controller

- **The main purpose of the Cluster Power Controller (CPC) is to manage static leakage and dynamic power consumption based on system-level power states assigned to the individual components of the Coherent Processing System.**
  - The CPC acts as a programmable platform peripheral, accessible through software and SOC level hardware protocols.
- **In addition to power control the CPC also controls the resetting of each processor.**

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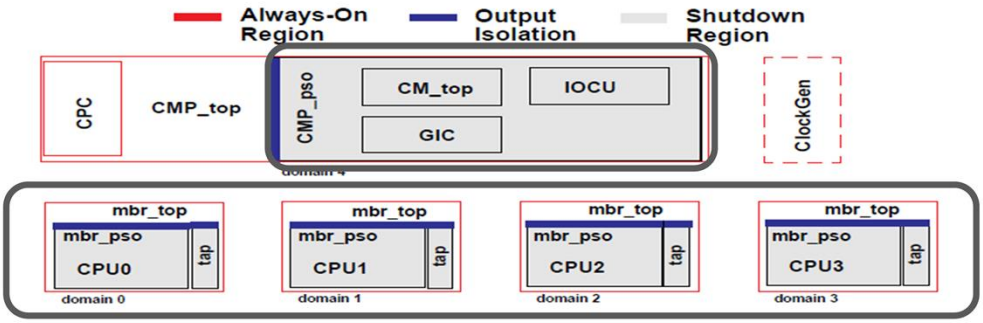
The Cluster Power Controller controls the power consumption in accordance with the system load. More processing elements can be powered up when needed and powered down when they are no longer needed.

The CPC is external to any core and global to the SOC. It can be controlled by any core and any core can use it to control another core.

The CPC also controls the resetting of the processors. For example on system power on a processor can be held in reset and latter started through the CPC.

Power Domains

- **A Coherent processing System can have up to 5 power domains.**
  - 1 to 4 Processor domains
  - 1 Coherency manager domain



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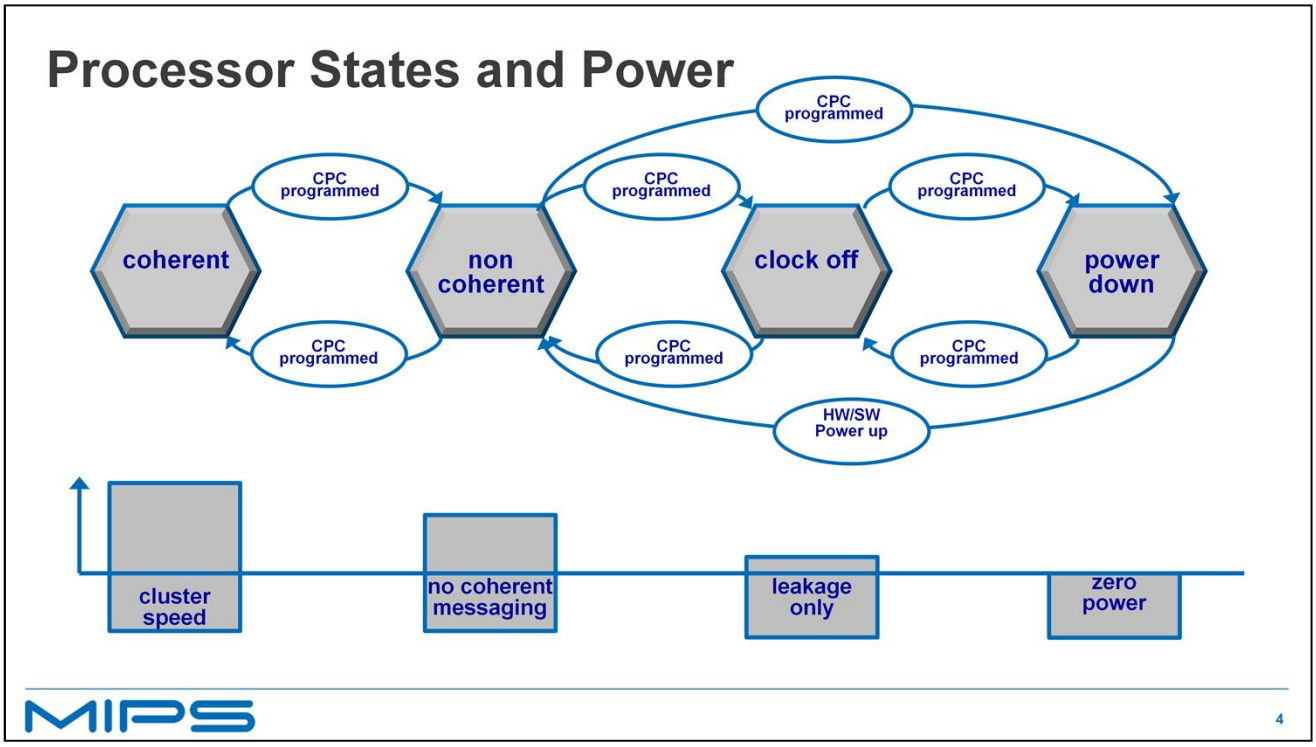
The cluster power controller breaks the coherent processing system down into isolated power domains. Domains that can shutdown are indicated in grey.

+ Each processor is in its own power domain

+ and the Coherency Manager is in its own domain.

Each processor domain can be controlled by software through the Cluster Power Controller Registers. With shutdown of all four cores and an inactive IOCU, the Coherence Manager becomes inactive and can be shutdown.



This slides shows the possible flow between Processor states along with some idea of power consumption.

The Coherent Processing System has 4 power states.

+ The processor is in a coherent state when a Processor is in a coherent domain. As I covered in the Global Control Register section, the coherent domain is set up by the GCR Core Local Coherence Control Register. In this state all things on the SOC are available to the Processor and its Processing Elements. The most power is used in this state.

+ In the non-coherent state when a Processor is not part of a Coherent Domain, the Processing Elements of the processor run as if they are in a single Processing System. This state will use a little less power then the Coherent state.

+ In the Clock off state the processor will not execute any instructions but the state of the processor is preserved. Before this state can be entered the processor must not be part of a Coherent Domain and all coherent transactions must be completed. There is significantly less power used in this state when compared to the Coherent and Non-Coherent states.

+ The power-down state is just that, the processor is off, processor state is not preserved. This state uses no power.

The next slides will cover the code sequence to go from one state to another.

Cluster Power Controller Base Address

- **Programmed by boot code**
  - Set in the GCR CPC Base register within the CM's Global Control Register Block

Register Fields		Cluster Power Controller Base Address Register (GCR_CPC_BASE Offset 0x0088)	Reset State
Name	Bits		
CPC_BaseAddress	31 - 15	Base address of the 32K Cluster Power Controller.	UD
CPC_EN	0	If set, the address region for the CPC is enabled. Cannot be set if CPC_EX = 0	0

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The address of the Cluster Power Controller registers should be programmed by the boot code into the GCR CPC Base register. This register is located within the Global Configuration Register Block at offset 88 hex.

As you can see from the table the address is on a 32K boundary so the lower 15 bits of the address will always be 0. This leaves space for additional information in the register. The CPC_EN field controls the enabling of the CPC. Once the boot code configures the CPC it should enable it by setting this bit. Before you do that you should make sure your system has a Cluster Power Controller by checking the GCR, Cluster Power Controller Status Register's CPC_EX field. If that field is a 1 then a CPC is attached to the CM. Since there are no other fields in the Cluster Power Controller Status Register and all other bits are Read only and reset to 0 you can just check the register for greater than 0.

VP Local GCR Other Register

This register is instantiated for each VP domain.

Register Fields		VP Local GCR Other Register (GCR_CL_OTHER,GCR_CO_OTHER) Offset: 0x0018	Reset State
Name	Bits		
CORE_OTHER	13:8	Sets "other core" when accessing a core-other sub-region	0 RW
VP_OTHER	2:0	Sets "other vp" when accessing a vp-other sub-region	0 RW

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The CORE_OTHER field of the “VP Local GCR Other Register” needs to be written with the number of the other core who’s local registers you wish to access. Once this is written you can access that CPU’s CM Local registers through the Core-Other register block.

The VP_OTHER field of the “VP Local GCR Other Register” needs to be written with the number of the other VP who’s local registers you wish to access. Once this is written you can access that CPU’s CM Local registers through the Core-Other register block.

Local Command Register

- **Leaving Coherent Domain**
  - Flush and Invalidate Caches
  - Clear COH_DOMAIN_EN in GCR Core Local Coherence Control Register

Register Fields		Local Command Register (CPC_CMD_REG, Offset 0x2000, 4000)	Reset State
Name	Bits		
CMD	3 - 0	0x0001 – ClockOff clock off, Power Down	0
		0x0010 – PwrDown Power down	
		0x0011 - PwrUp - Other access PWRUP_EVENT dependent	
		0x0100- Reset Reset domain, Power up state	

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The Command register is located in the Local and other Blocks of the CPC registers at offset 2000 hex for the local Command register and 4000 hex for the Other local Command register.

The only field in this register is the 4 bit command field. Each command can change the state of a processor depending on conditions within the CPS.

+ To issue any of these commands the target processor must not be in a Coherent domain. If the target processor is in a coherent domain the command will have no effect until the processor leaves the coherent domain.

+ If a processor is in a Coherent Domain it must first flush and invalidate all cache lines in the Processor.

+ Then it can remove itself from the Domain by clearing the GCR Local Coherence Control Register. Clearing this register Disables interventions from other cores and removes the processor from the Coherent Domain. On top of this, the OS may require the saving of the processor state especially if the processor is going to be powered down.

+ The Clock Off command brings the processor from a non-coherent state to a clock off state where nothing is executing on the processor but the processor state is preserved.

+ The Power Down command can be done when the processor is in a non-coherent state or a Clock Off state. It will power off the processor completely.

+ The Power up command obviously can only be done from another processor writing to the targets command register using the CPC Core Other section. The execution of this command depends on the previous domain power state. If the domain is powered down, a Power Up command will enable power for the domain and bring the domain into operational state of non-Coherent execution. However, when bringing a domain up after a Power Down command is executed, the Reset command is generally preferable to Power Up. A reset will always insure a clean start irrespective of the current state.

If the previous power domain state was Clock Off, a Power Up command will raise the domain state to either non-coherent or coherent operation, dependent on the GCR Local Coherence Control Register settings.

+ The Reset Command allows a domain in non-coherent operation to be reset. It also can be sent to a domain in power-down or clock-off mode. The domain will then become active, and a reset sequence is executed which leads to an operational state of non-coherent or coherent dependent on the GCR Local Coherence Control Register.