Teaching Materials: MIPSfpga v2.0

Introduction

It has become the benchmark for Teaching Computer Architecture, and a vital reference for students learning to design Systems-on-Chip. After two years of experience with more than 600 licenced users, we have refined and extended MIPSfpga into v2.0. Version 2.0 is an evolution from v1.3 and brings a rich set of additional exercises as well as many small improvements to make the system easier to use. The UDI instructions in the core are now enabled, and Fast Debug Channel (FDC) is also enabled. MIPSfpga v2.0 is not a replacement for previous versions, but an extension of them. MIPSfpga provides the RTL source code of the MIPS microAptiv UP core for implementation on an FPGA, together with extensive teaching materials. The MIPS microAptiv UP core is a member of the same microcontroller family found in many embedded devices, including the popular PIC32MZ & PIC32MK microcontrollers from Microchip and the Artik 1 from Samsung.

The teaching materials show you how to use this core as part of a Computer Architecture course, paving the way for your students to explore how a commercial pipelined processor core works inside and to use this core in their projects, in effect creating their own SoC designs.

With its long heritage and excellent documentation, MIPS is the preferred choice of RISC architecture for many teachers around the world. But in the past, to demonstrate key concepts, teachers had to settle for creating partial ‘MIPS-like’ cores or using unofficial copies of dubious heritage. Not now - MIPSfpga is the real ‘industrial’ RTL, non-obfuscated, and available freely for academic use.

Structure

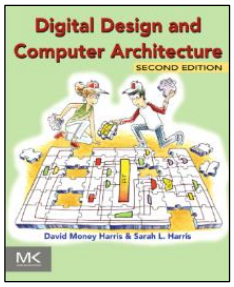
The MIPSfpga teaching materials consist of three parts:

- **MIPSfpga Getting Started** contains a detailed guide that begins with a brief introduction to the MIPSfpga core, which is included in the package. It gives an overview of how to setup the core for simulation or putting it on to an FPGA, as well as programming the processor. Guides on software installation, both for Windows and Linux systems are also given, along with detailed reference guides about the core and its ISA – Instruction Set Architecture, the System Integrator’s Guide and how to use the UDI – User Defined Instructions. **All users need this package** because it contains the RTL, the reference guides, an OpenOCD + Codescape Essentials Installer and a number of other components. The “Getting Started Guides” in other languages are just translations of the guide on its own.
- **MIPSfpga Labs**. MIPSfpga v2.0 increases the number of lab exercises from the original 9 to 25. In this package you will find slides with accompanying lab scripts, illustrated using the Digilent Nexys 4 DDR and other platforms. In the first part of these labs you will be taken from building the core, to programming in both C and assembly. You then progress to adding a range of peripherals to the core to enable a greater level of interaction, and to use interrupts and a DMA for Input/Output. Instructions on how to port MIPSfpga to other FPGA boards (such as Basys 3 and DE2-115) are also provided. The third part of this package includes several in-depth labs about the core internals, where you will analyse and modify the pipeline, and two labs where use the Performance Counters and the MIPS CorExtend Interface. Finally, you study the memory system of MIPSfpga.

- **MIPSfpga SOC.** This advanced package enables you to run Buildroot Linux on MIPSfpga specifically using the Digilent Nexys4 DDR platform. The microAptiv core is packaged as an IP block usable by Xilinx's Vivado IP Integrator. As a result, AXI based IP blocks from Xilinx can easily be interfaced with the MIPS core. These are used to create an example SoC, such as a design with a UART and Ethernet, running under Linux, on MIPSfpga. A custom AXI GPIO block along with an example Linux driver is also provided. There is extensive documentation included. Collectively these provide an excellent basis for a SoC course that is highly relevant to the needs of the chip design industry, although the level of complexity makes this a postgrad class. PhD students and Postdocs will find this material very useful for research projects.

Target Courses & Projects (Education Level)

- Digital Design & Microarchitectures (BSc)
- Computer Organisation & Architecture, Advanced Computer Architecture (BSc, MSc)
- SoC design (MSc)
- Design Verification (MSc)
- Embedded Systems projects (BSc, MSc)
- Processor Architecture: modifications, enhancements, optimisation…(MSc, PhD)



The Authors

The v1.3 course materials were developed by David Harris and Sarah Harris, co-authors of the popular textbook Digital Design and Computer Architecture which provides a uniquely relevant accompaniment to MIPSfpga. For v2.0 Sarah Harris was joined by Daniel Chaver, Yuri Panchul, and Bruce Ableidinger. Zubair Kakakhel wrote SoC, with editing by Sarah Harris and David Harris.

Complementary Materials

- The textbook 'Computer Organisation and Design' by David Patterson and John L. Hennessy remains the 'bible' for these activities, and provides further depth to Harris & Harris in a MIPSfpga-based course.
- Other relevant textbooks are referenced here:
- Access the microAptiv core in silicon through boards such as Digilent's 'WiFire' incorporating Microchip's PIC32MZ MCU.
- Videos of the workshop given by Sarah Harris and Parimal Patel of Xilinx is online here: http://community.imgtec.com/university/video-gallery/
- Our global Workshop Schedule Programme is regularly updated at University Events

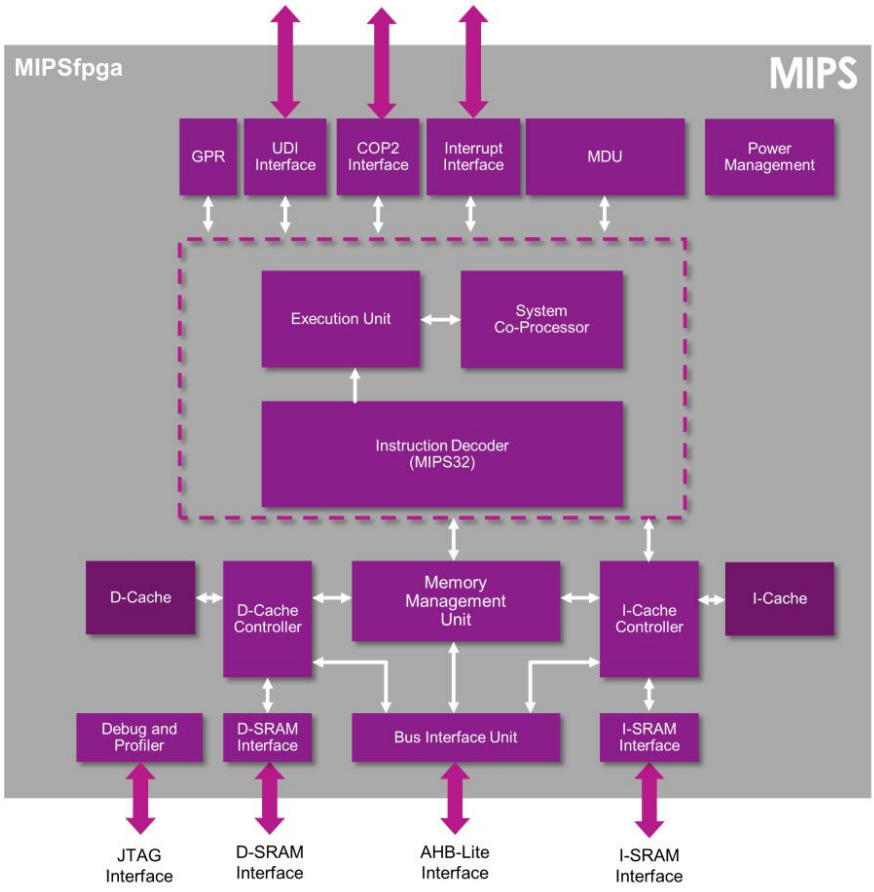
Required Tools

Hardware
• Host PC: 64-bit Windows or Linux operating systems • Digilent Basys 3 or Nexys 4 DDR, with Xilinx Artix 7 FPGA • Users have shown porting to other boards such as: Zed, Nexys 3, Nexys 4 (not DDR), DE-0 nano, and DE2-115. • JTAG Probe: SEEED Studio MIPS Bus Blaster including 14 to 12 pin adaptor for the Nexys4 DDR board

Software (all free-of-charge)
• Codescape MIPS SDK Essentials (Installer included with Getting Started Package) • OpenOCD (Installer included with Getting Started Package). Or use the offline version download from the IUP website, Teaching Resources section • Vivado (Xilinx) Web Pack edition • Mentor Graphics ModelSim (Student or Full editions) or Xilinx Xsim

Core Structure

The core is approximately 40K gates.



Availability

MIPSfpga Getting Started Guide v2.0, MIPSfpga Labs v2.0, MIPSfpga SoC ver. 1.0

Languages for MIPSfpga v2.0:

- English: now
- Russian & Simplified Chinese: Q1'18

Languages available now for MIPSfpga v1.3:

- Simplified Chinese, Japanese, Russian, Spanish

Support

- The MIPSfpga forum is specifically for technical questions about MIPSfpga
- The IUP (Imagination University Programme) forum here for curriculum and other discussions

Partners

We have worked closely with Xilinx and Digilent who have given wonderful support to this large and complex project. You can visit their University Programmes are here:

XILINX | UNIVERSITY PROGRAM

DIGILENT A National Instruments Company

User Licenses

- Simple, online, and easy to understand…
- For the **MIPS core**:
  The agreement is part of the Getting Started Package download process, and acceptance is required before the download request can be submitted.
  The End User Licence Agreement (EULA) allows the use of the MIPS core on FPGA platforms for the academic purposes of teaching, student projects and research. It allows teachers to distribute the core to students in classes, and it allows for the core to be modified. It does not allow the core to be put into silicon. Furthermore, if the core is modified and the user wishes to patent these modifications, the licence requires that this is negotiated with Imagination first.
  The EULA is written in plain English, and a copy of the EULA is part of the Getting Started package for future reference.
- For the **Teaching Materials**:
  The agreement is part of the Fundamentals and Advanced download process.
  The End User Licence Agreement (EULA) explains that the materials are for Educational and Non-Commercial use, which means that companies or trainers who wish to use the materials for paid-for training, must seek Imagination's prior permission. Distribution of the materials to your Students is expressly allowed. The agreement allows extracts of the material to be used in derived teaching materials as long as Imagination's copyright is acknowledged, but publication in textbooks needs prior permission (which is usually given). No warranty is provided as to the effectiveness of the materials. The EULA is written in plain English, and a copy of the EULA is included in the materials package for future reference.

"MPW" – Routes to Silicon

We have authorised Europractice to licence the Warrior M class core for use in silicon runs of up to 100 units, for Academic Institutions in Europe, the Middle East, Africa, and Russia.
MOSIS provide a similar service in the US, Canada, Japan, Korea, Singapore, China, Brazil and others.

EUROPRACTICE

The MOSIS Service

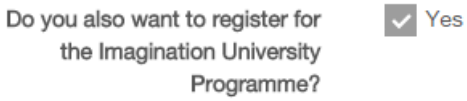
Empowering Academia from Theory to Silicon: The knowledge of how a MIPS works, through a soft-core for FPGA use, and to silicon for research projects. The complete spectrum!

Press Releases/Blogs/Papers:

- Free and Open Access to a Modern MIPS CPU
- MIPSfpga programme opens up the MIPS architecture to universities worldwide
- Imagination expands the scope of its university program with groundbreaking EUROPRACTICE partnership
- MIPSfpga v2.0: Press Release click here
- ISCA 2017 WCAE Conference: "Practical Experiences Based on MIPSfpga"

How to join the IUP and access these materials

1. Click 'Register' or 'Join IUP' on the landing page: www.imgtec.com/university
2. Complete the first section: 'the Community Registration'
3. Tick the box marked 'Join Imagination University Programme' and complete the additional information



4. A verification email will be sent to your inbox for activation.
   (Please also check your spam mailbox because occasionally the mail gets filtered)
5. To download teaching materials, visit the IUP page – Teaching Resources
   http://community.imgtec.com/university/resources/
6. Request the package(s) you want, accept the Licence Agreement, and give some details about how you plan to use the materials.
7. We then receive a request to approve the download, and normally action this within 48 hours. Once approved, you will receive an e-mail saying you can now make the download.

NOTE: Requests may be rejected for the following reasons:
- The registration details are incomplete
- There are few or no details of intended use
- The requester appears to be a commercial company or a competitor

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