
This is the MIPS by Imagination Multi Threading Training Course

# Introduction

- This class covers additions to the MIPS Architecture that are implemented for the MT Processor Core.
- A prerequisite to this training is the programming a MIPS core.

MIPS



This section covers the additions to the MIPS architecture for the MT/ASE as it pertains to a MT processor

+ A prerequisite to this training course is the programming a MIPS core class.

## Introduction

- This course is designed for Software Engineers.
- A working knowledge of Multi Threading, such as POSIX threads is assumed.

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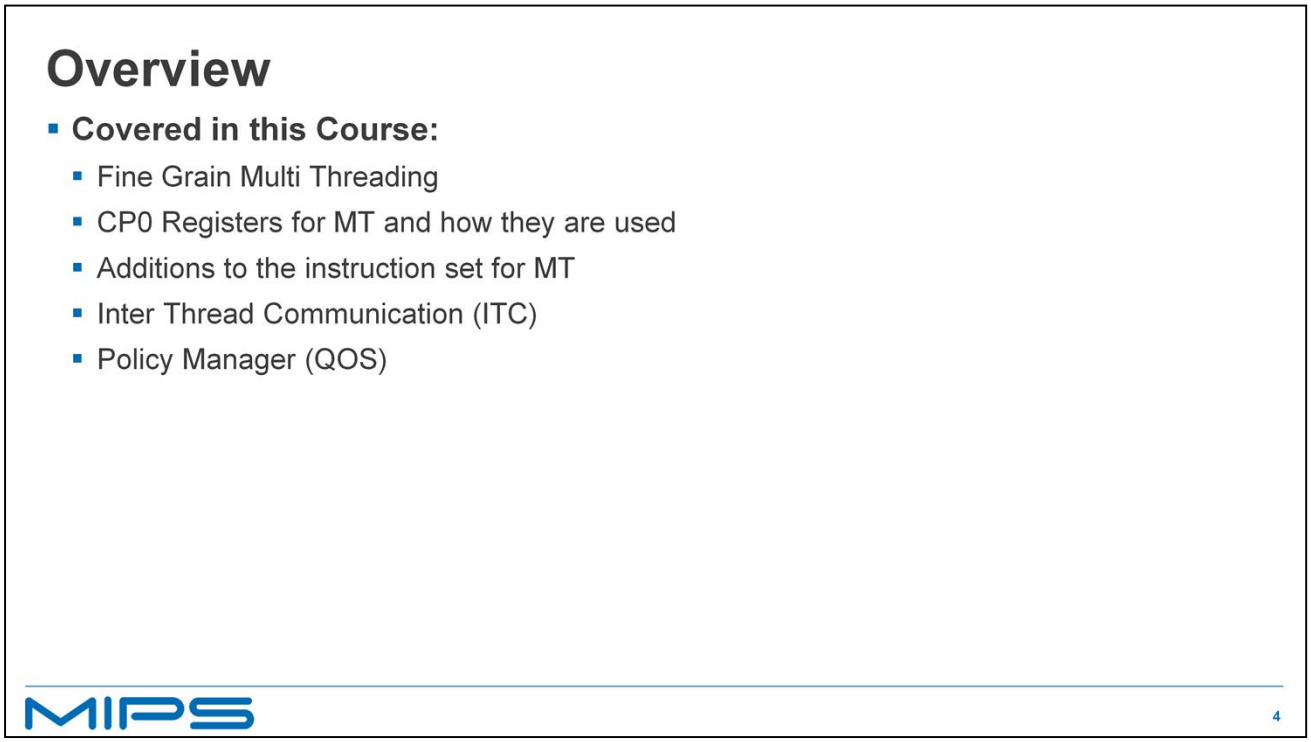
This course was designed for software engineers with a working knowledge of multithreading such as POSIX threads.




In this course we will cover

+ Fine-grained multithreading

+ CP0 registers for multithreading

+ The additional instructions that were added to the instruction set for multithreading

+ Inter-thread communications for communicating between threads

+ and the policy managers which are used to schedule the quality of service for each thread