This is an overview of the “Programming A MIPS Core” software class

Course Contents

- **This is a software class for programmers who are not familiar with MIPS cores or development tools.**
- **It will give you an in-depth view of MIPS specific programming needs.**
- **It will go in-depth into:**
  - The MIPS instruction set, assembly language coding, the MIPS memory map, programming a TLB, exceptions and interrupts, caches, scratch pad RAM, CPU initialization code, power management, and MIPS specific C. porting needs.

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This class covers software topics related to MIPS Technologies CORES.

+ It is tailored to meet the needs of software engineers who are not familiar with MIPS Cores or the development tools offered by MIPS.

+ You will be given an in-depth view of MIPS specific programming needs for system programmers

+ that includes programming Caches, TLB, Exceptions and more.

Instruction Set Section

- **This section covers the MIPS64 Release 6 instruction set**
  - Instructions will be broken down into 2 types of instructions:
    - Machine instructions – These instruction are directly defined by the MIPS Architecture specification.
    - Macro instructions – instructions that are aliases for actual machine instructions or instructions that the assembler will translate into multiple machine instructions.

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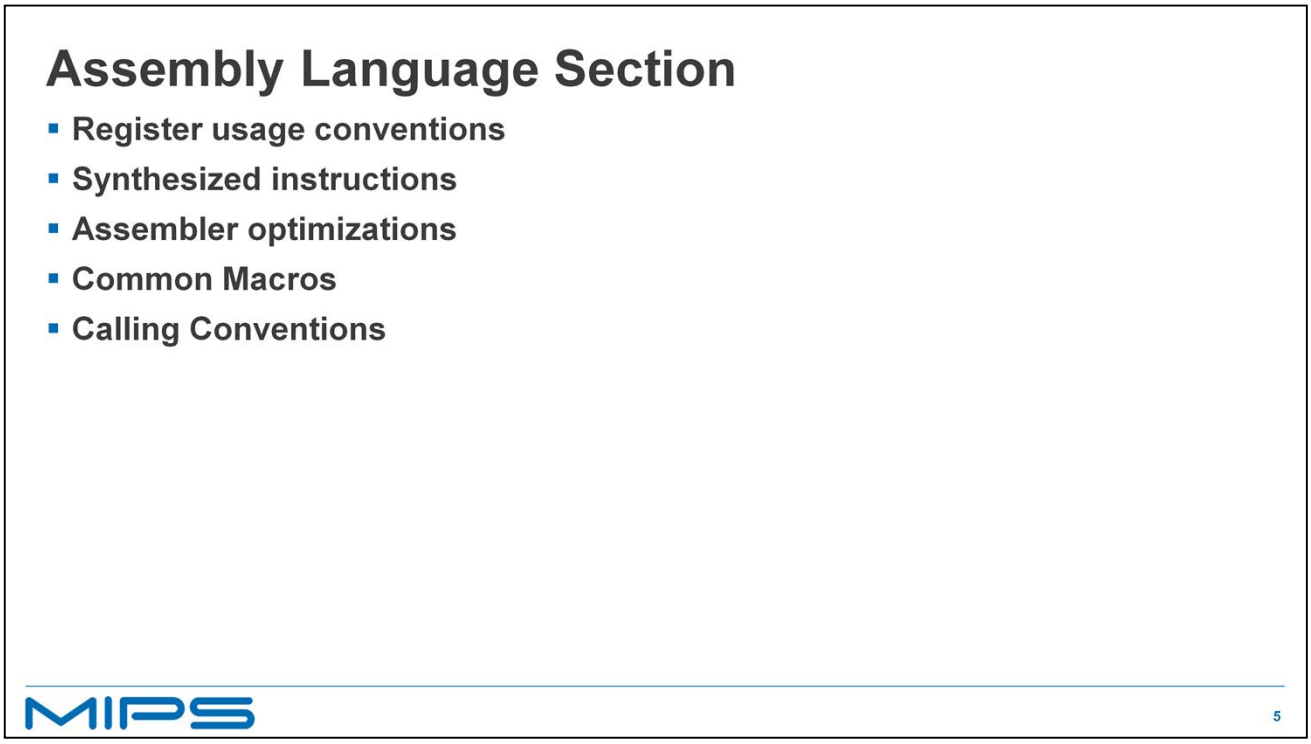
The instruction set section covers the MIPS64 release 6 instruction set

+ It does so by breaking down the instructions into two types.

+ First a machine instruction which is directly defined in the MIPS architecture and has a one to one correspondence with a single instruction bit encoding.

+ And second there are macro instructions. These instructions are supplied by the assembler to make assemble coding easier. These instructions can be a simple as an alias to a machine instruction or translated into a series of machine instructions.



The assembly language section covers

+ the usage conventions for the 32 general purpose registers
+ synthesized instructions
+ assembler optimizations
+ Common macros you can use
+ Function Calling conventions

Memory Map Section

- Memory Map with TLB
- Memory map view at exception time and boot up
- MIPS64 memory map

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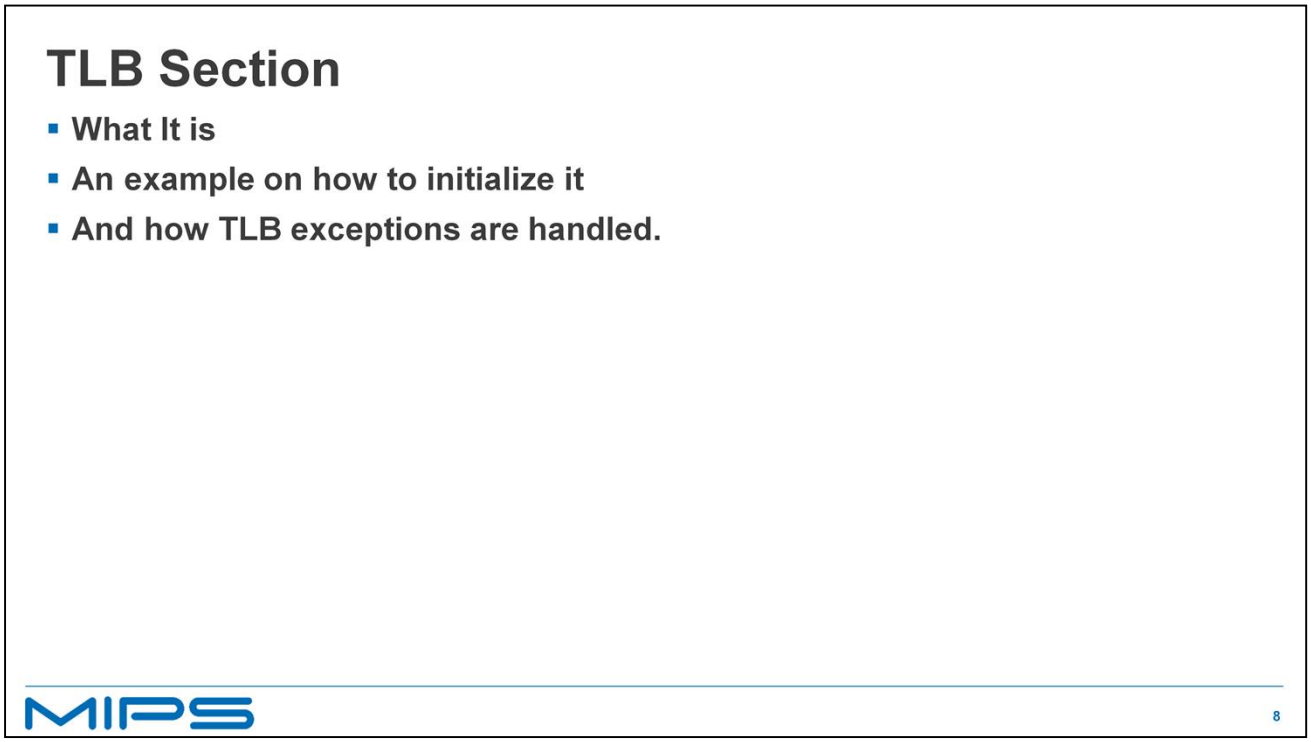
The MIPS architecture has a very defined way in which the CPU views memory. The memory map section will go into the MIPS privileged resource architecture. In this architecture the CPU view of memory changes depending on what state the CPU is in and how addresses are being translated.

+ This section covers the memory map with a TLB or translation lookaside buffer.

+ The memory map with FMT or fixed map translation.

+ The class will go into what the memory map looks like at exception time and boot up.

+ I will cover the Memory map in 64 bit mode



The next section will cover the Translation Look aside Buffer or TLB

+ It will cover What the TLB is
+ How to initialize the TLB including a programming example.
+ And how TLB exceptions are handled.

Exceptions and Interrupts Section

- What is an exception
- What exceptions are generated by the MIPS core
- Different ways interrupts can be handled such as vectored interrupts or external interrupt controllers.
- An example of an interrupt using shadow register sets an example that doesn't use a shadow register set.

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In the exceptions and interrupts section the class will cover

+ what an exception is

+ And what exceptions are generated by a MIPS core.

+ Then the class will go into a specific form of an exception called an interrupt. The class will go into the two different interrupt modes, vectored interrupt mode or external interrupt controller mode they can be used to access the interrupt code.

+ This section will also go over an interrupt code example that uses a general-purpose registers and one that uses a shadow register set feature.

Cache Section

- Cache dimensions
- Cache Lookup
- Cache policy
- Non-blocking loads
- Cache initialization example code
- Cache management
- Virtual aliasing
- Prefetching of data and instructions
- Cache exceptions

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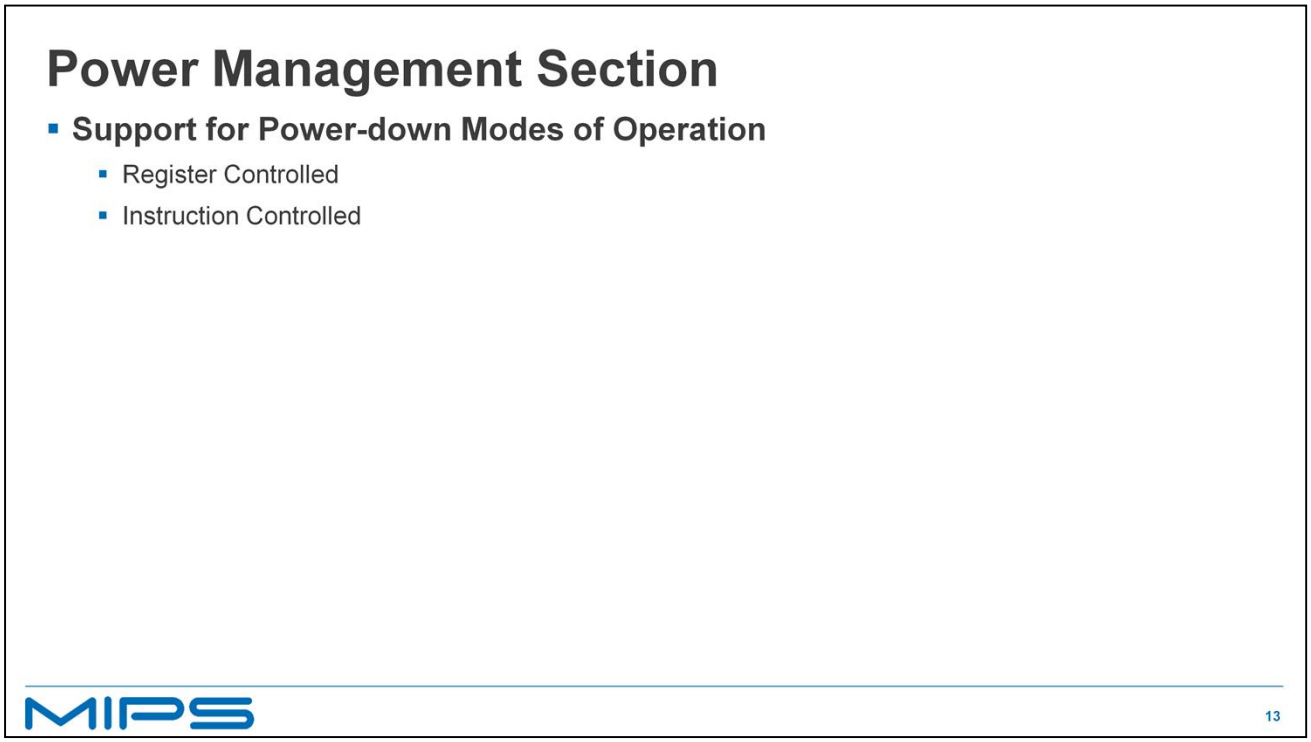
The Cache section will cover

+ The Dimensions of the cache and what make up the size of the cache
+ how things are looked up in the cache
+ what types of cache policy you can set
+ What non-blocking loads are
+ The initialization of the cache
+ cache management such as cache flushing
+ what virtual aliasing is and how to avoid it
+ what the prefetch instruction does
+ cache exceptions



The CPU core boot up section of the class gives you a coding example for what needs to be initialized for a MIPS core.

Porting C Programs Section

- **Common Problems**
  - Which end of the egg to eat? (Endianness)
  - Caches and Physical Memory Map
  - Data Alignment
  - Short Variables
  - Unsigned Characters
  - Bit Fields

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The CPU core boot up section of the class gives you a coding example for what needs to be initialized for a MIPS core.