Meet the MIPS I-class I6500-F
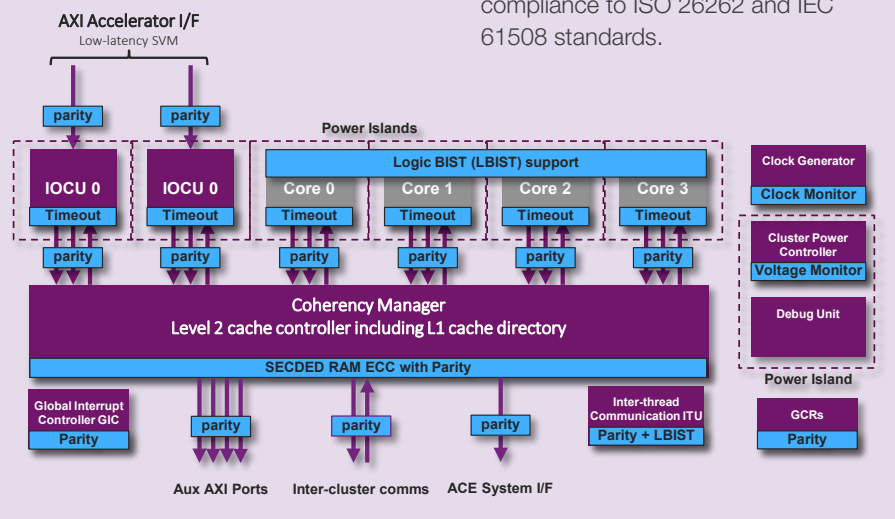
CPU IP designed for safety critical systems in an autonomous age

MIPS I-class I6500-F key features/benefits:

Safety compliant work products:

- Designed with rigorous QMS processes and safety methodology for addressing systematic and random failures.

- SEooC design, with optimised safety measures for ASIL B[D] design.

- Independently assessed for formal compliance to ISO 26262 and IEC 61508 standards.

Heterogeneous Inside & Out:

- Each CPU in a single cluster can be configured with different combinations of threads, cache sizes, frequencies, and even voltage levels.

- IOCU ports enable optimised, low-latency integration of accelerators with shared virtual memory (SVM).

- The latest MIPS Coherence Manager with an AMBA® ACE interface to popular ACE coherent fabric solutions lets designers mix configurations of processing clusters on a chip for high system efficiency.

Simultaneous Multi-threading (SMT):

- Hardware multi-threading enables execution of multiple instructions from multiple threads every clock cycle, providing higher utilization and CPU efficiency.

Security and Reliability:

- security technology enables isolation of critical assets from potential hazards, and can provide support for a trusted execution environment where trusted applications can reside.

Hardware virtualization (VZ):

- Designers can save costs by safely and securely consolidating processes that might have run on multiple CPU cores in the past with a single core today, save power where multiple cores are required, and dynamically and deterministically allocate CPU bandwidth per application.

SMT + VZ:

- The combination of SMT with VZ offers "zero context switching" for applications requiring real-time response; alongside the provision of scratchpad memory this makes I6500-F ideal for applications which require deterministic code execution.

Features for compute-intensive data processing and networking applications:

- Data scratchpad memories per CPU and features for fast path message/data passing between threads and cores enable high-performance/high-efficiency data transfers to localized compute resources.

Broad development ecosystem:

- A wide selection of available compilers, debuggers, operating systems, hypervisors and application software – all optimized for MIPS – enables straightforward software development.