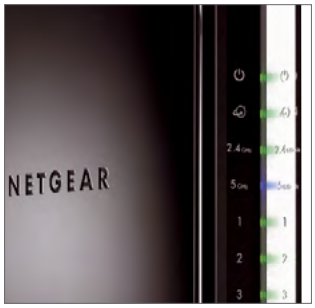
MIPS
by Imagination

Microprocessors




Imagination

Imagination Technologies – a trusted IP partner

Imagination is a global technology leader whose products touch the lives of billions of people throughout the world. The company's broad range of silicon IP (intellectual property) includes the key multimedia, communications and general purpose processors needed to create the SoCs (Systems on Chips) that power all mobile, consumer, automotive, enterprise, infrastructure, IoT and embedded electronics. These are complemented by its unique software and cloud IP and system solution focus, enabling its licensees and partners get to market quickly by creating and leveraging highly differentiated SoC platforms.

About MIPS CPUs

Based on a heritage built and continuously innovated over more than three decades, Imagination's MIPS® architecture is the industry's most efficient RISC architecture, delivering the best performance and lowest power consumption in a given silicon area. SoC designers can use this efficiency advantage for significant cost and power savings, or to implement additional cores to deliver a performance advantage in the same power, thermal and area budget.

Imagination's family of MIPS processor cores are ideal for products where ultra low-power, compact silicon area and a high level of integration are required.

Our powerful, yet flexible CPU IP scales seamlessly from entry-level to high-end, and features advanced technologies such as hardware multi-threading, compatible 32-bit and 64-bit instruction set architectures (ISAs), and ISA consistency from entry-level to high-end.

MIPS is one of only three CPU architectures officially supported by Google's Android, making it ideal for Android-based devices, as well as a wide range of other OS including Linux, and a range of RTOS (real-time OS). With billions of MIPS-based products already shipped, and many universities and schools around the world teaching CPU architecture using MIPS as their preferred platform, MIPS is truly the ideal CPU for tomorrow's SoCs, from the highest-performance mobile applications processors to the lowest power connected sensor processors.

MIPS Architecture

The market-leading MIPS architecture was created in the early 1980s as a 32-bit RISC processor focused on providing the highest levels of performance together with new levels of silicon efficiency thanks to its clean, elegant design. MIPS CPUs deliver lower power consumption and smaller silicon area than other CPUs thanks to an extremely well-defined, clean RISC architecture coupled with many years' experience in the most demanding environments from networking to TVs and set-top boxes.

MIPS is a simple, streamlined, highly scalable RISC architecture that is available for licensing. Over time, the architecture has evolved, acquired new technologies and developed a robust ecosystem and comprehensive industry support. Its fundamental characteristics – such as the large number of registers, the number and the character of the instructions, and the visible pipeline delay slots – enable the MIPS architecture to deliver the highest performance per square millimetre for licensable IP cores, as well as high levels of power efficiency for today's SoC designs.

MIPS Architecture Products

- The MIPS32® and MIPS64® instruction-set architectures are seamlessly compatible and allow customers to port from one generation to the next while preserving their investment in existing software.
- microMIPS® is a code compression ISA comprised of 16 and 32-bit instructions that provides similar performance to MIPS32 with a code size reduction of up to 35%.
- Architecture modules that provide a range of flexible, scalable and powerful options include:

  Multi-threading – can make a single processor core appear and function like multiple separate cores for improved performance and efficiency.

  SIMD (Single Instruction Multiple Data) – improves performance by allowing efficient parallel processing of vector operations.

  Virtualization – provides enhanced security features and support for multiple operating systems.

  DSP Technology – supporting the growing number of consumer products which require an increasing amount of signal and media processing horsepower.

- Application-specific extensions (ASEs) that boost performance for specific types of applications include:

  SmartMIPS™ ASE enables security in smart cards and other secure data applications.

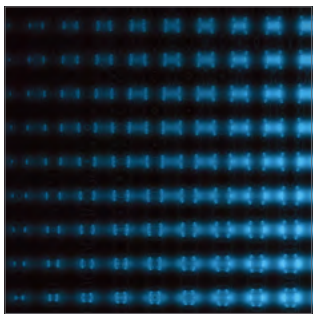
  MIPS16e™ code compression ASE reduces memory requirements by as much as 40%.

  MIPS-3D™ ASE provides a cost-effective and an efficient way to achieve high-performance 3D geometry processing within the context of a MIPS64 architecture.

  MIPS MCU ASE provides enhanced handling of memory-mapped I/O registers and lower interrupt latencies.

	SIMD	Virtualization	Multi-threading	DSP	MIPS16e™ ASE	SmartMIPS ASE	MIPS-3D ASE	MCU ASE
MIPS32	●	●	●	●	●	●	●	●
MIPS64	●	●	●	●	●		●	●
microMIPS32	●	●	●	●		●		●
microMIPS64	●	●	●	●			●	●

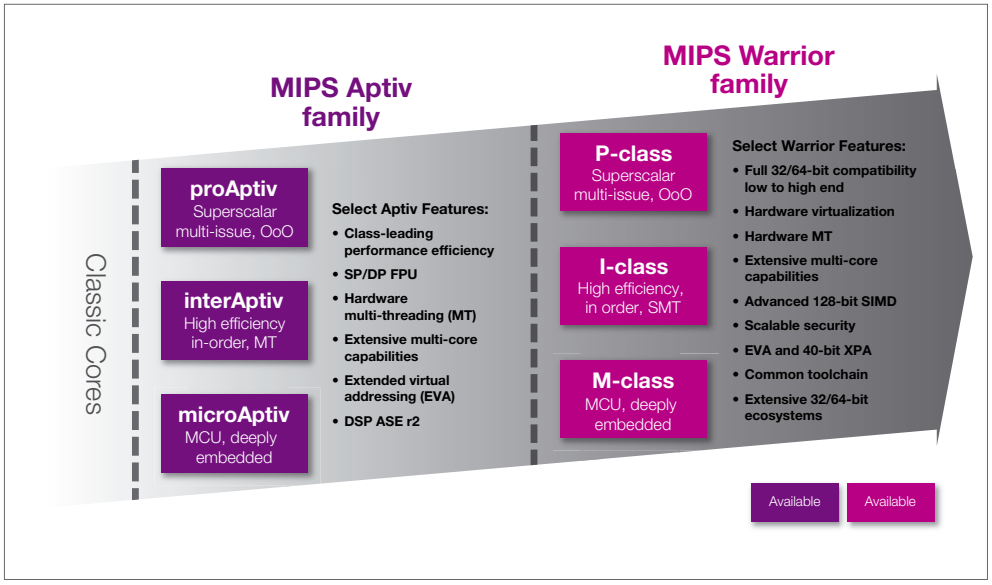
The MIPS architecture is one of the most widely supported of all processor architectures, with a broad infrastructure of standard tools, software and services to help ensure rapid, reliable, cost-effective development. Microprocessor developers who want maximum flexibility from processor IP have a solution in the MIPS architecture.



MIPS Processors

MIPS comprises a broad array of low-power, high-performance embedded microprocessor cores that power billions of products around the globe. MIPS processors are ideal for next-generation embedded designs across numerous high-growth markets, including digital consumer, mobile, broadband access and networking, state-of-the-art communications and more. To address the myriad unique design needs of these markets, synthesizable MIPS processor cores range from entry-level to some of the industry's highest performing multiprocessors.

MIPS Roadmap



> *"Thirty years ago when we created the MIPS architecture, we embraced a new philosophy of computer design, with a focus on efficiency and simple extensible design principles. RISC was an important innovation in computer architecture, and I am pleased to see the continued innovation and development of the MIPS RISC architecture over the years. The initial simplicity and flexibility has enabled the architecture to grow and incorporate new architectural concepts, enabling MIPS to become one of the leading embedded architectures today."* ***—John L. Hennessy, Office of the President, Stanford University (Co-Founder, MIPS Computer Systems, 1984)***

MIPS Warrior Cores

In August 2013, Imagination announced the new MIPS Warrior CPU cores. These cores incorporate new architectural features and provide best-in-class performance and efficiency for a wide range of applications.

The Warrior generation of cores includes 32-bit and 64-bit variants with a focus on superior performance efficiency across the high-end, mid-range and entry-level/microcontroller CPUs. Building on the true 32-bit and 64-bit instruction set compatibility of MIPS, Warrior cores provide binary compatibility from the entry-level 32-bit microcontroller to the high-end 64-bit microprocessor. 64-bit Warrior cores have no need for a wasted logic legacy decoder to execute existing 32-bit code, and the broad range of tools and applications built for the 64-bit MIPS architecture over more than 20 years will seamlessly work with Warrior cores.

Key Warrior features include:

- Hardware virtualization across the entire range of cores, providing compelling benefits for applications from compute-intense enterprise environments to energy efficient mobile platforms.
- MIPS hardware multi-threading technology, enabling better overall throughput, quality of service (QoS), and power/performance efficiency in select Warrior cores.
- Imagination's unique, extensible and highly scalable security framework for applications including content protection on mobile devices, secure networking protocols and payment services.
- MIPS SIMD architecture, built on instructions designed to be easily supported within high-level languages such as C or OpenCL for fast and simple development of new code, as well as leverage of existing code.
- A consistent and comprehensive toolchain across the Warrior series for fast, easy development and debugging.

The CPU IP cores comprising the MIPS Warrior family comes in three classes of performance and features:

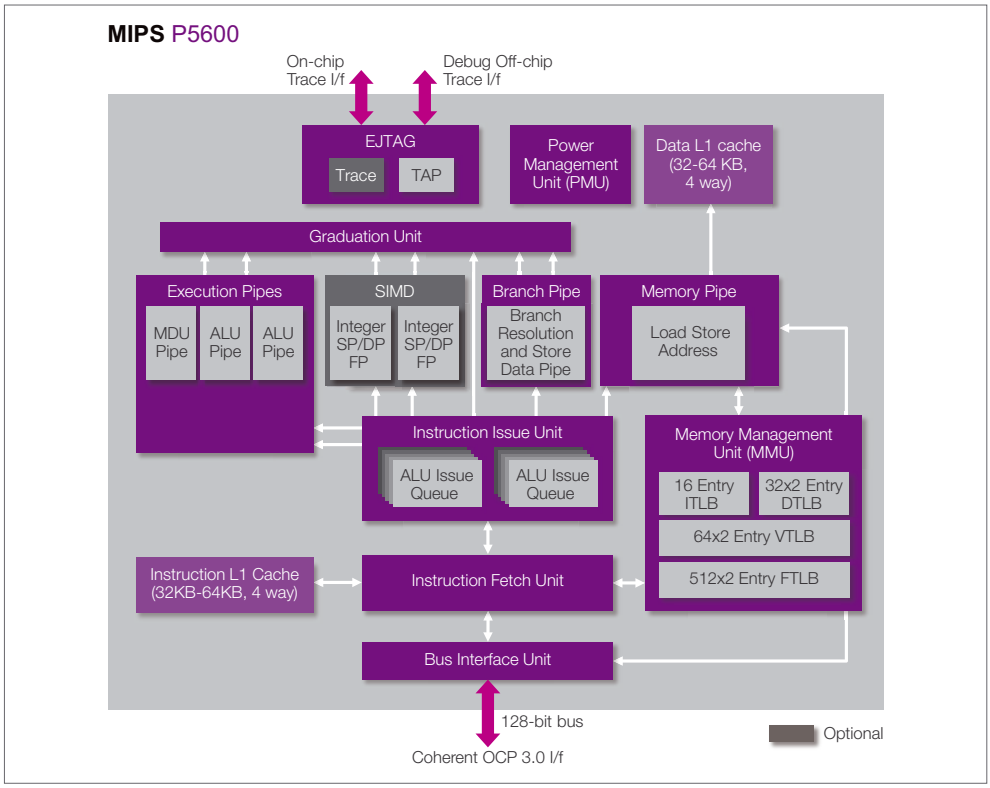
- 'Warrior M-class': entry-level MIPS cores for embedded and microcontroller applications, a progression from the popular microAptiv family
- 'Warrior I-class': mid-range, feature-rich MIPS CPUs following on from the highly-efficient interAptiv family
- 'Warrior P-class': high-performance MIPS processors building on the award-winning proAptiv family

Warrior P-class

P5600

The ‘Warrior P-class’ P5600 represents a major step forward in feature set for high-performance MIPS CPU IP cores. The P5600 core delivers industry-leading 32-bit performance together with class-leading low power characteristics in a silicon footprint up to 30% smaller than comparable CPU cores, making it ideal for a wide range of mobile, consumer and embedded applications.

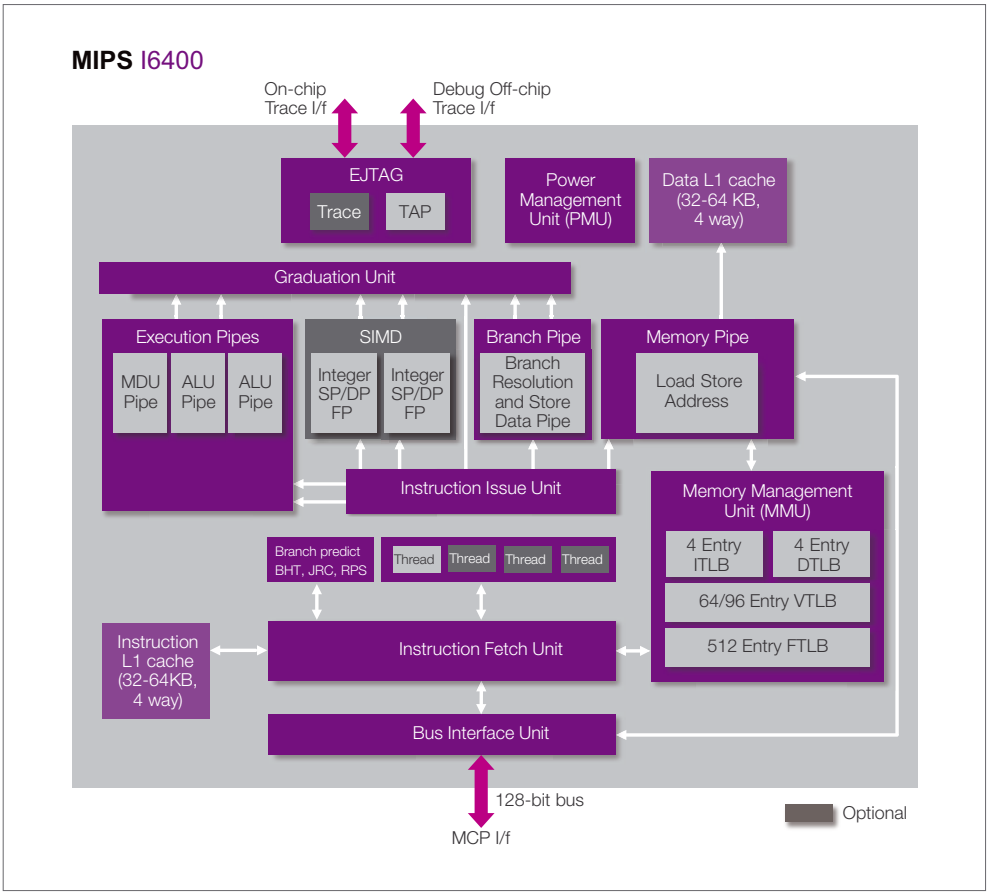
The MIPS P5600 incorporates key features needed for today’s leading-edge processors, including full 128-bit SIMD; simple, flexible and complete hardware virtualization; next-generation security; support for up to six cores per cluster with high-performance cache coherency; and other features including two different advanced addressing extensions which extend the usability of the P5600 well beyond other 32-bit CPUs.



Warror I-class

I6400

MIPS I6400 is the ultimate balance of performance with area and power efficiency. I6400 is built upon the proven 9 stage with dual-issue, in-order pipeline married with multi-threading technology. I6400 delivers scalable performance from a single virtual core to up to four virtual cores per physical core. It allows SoC designers to select the right performance for their silicon budget. Incorporating the advanced features of P5600, such as load store bonding and SIMD, I6400 is ideal as a mobile application processor and for networking applications that require optimal performance while managing silicon and power budget.



Warrior M-class

M51xx

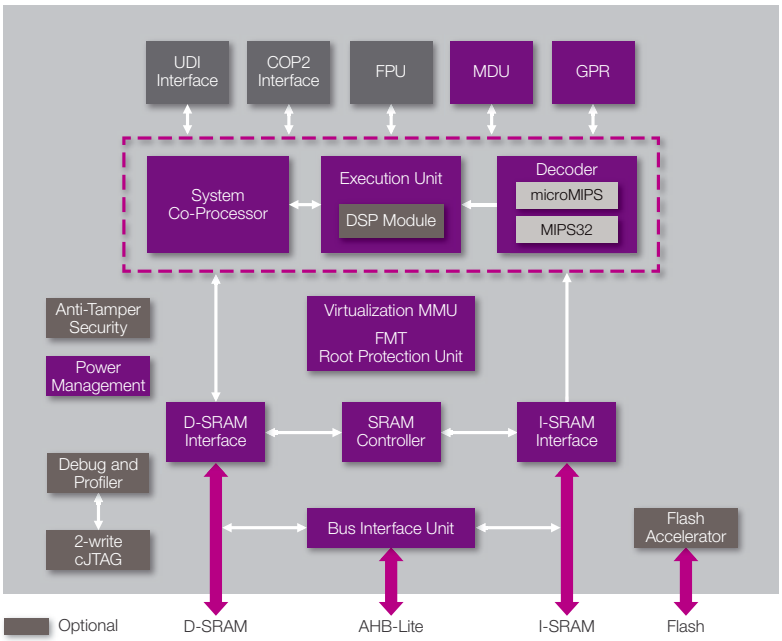
MIPS M51xx 'Warrior M-class' IP cores are the first microcontroller-class CPUs with hardware virtualization, bringing a new level of security and reliability to a wide range of entry-level embedded applications.

The M51xx cores maintain the high performance, comprehensive DSP/SIMD features of the previous generation MIPS microAptiv family of cores, along with the microMIPS Instruction Set Architecture (ISA), which provides up to 30% code size reduction over 32-bit only code.

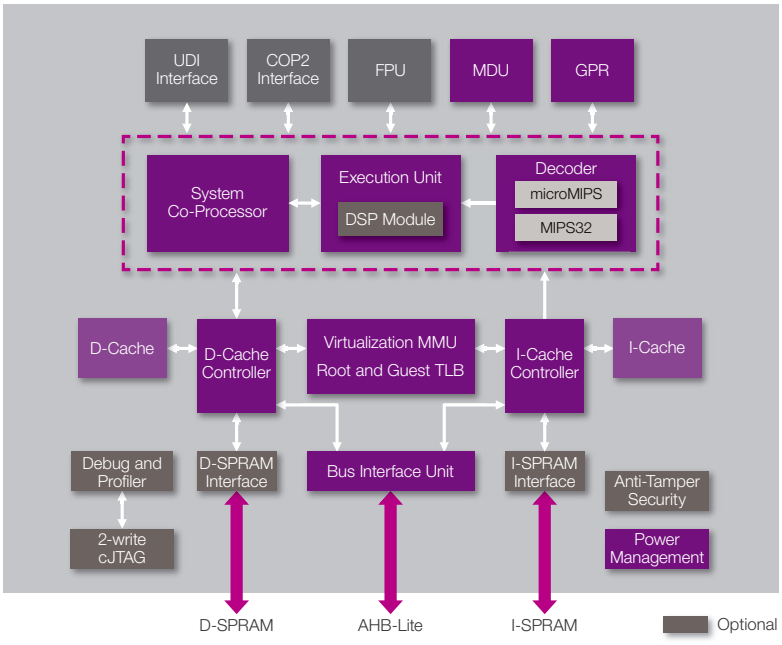
The first available M-class cores are the M5100 and the M5150. The M5100 integrates a real-time execution unit and SRAM controller, and is optimized for low-cost, low-power microcontroller applications. The M5150 adds a programmable L1 instruction and data cache controller, plus memory management support for high-performance Linux applications. An optional IEEE 754 Floating Point Unit provides high-performance support of both single and double precision instructions.

The M51xx cores are ideal for industrial control, Internet of Things (IoT), wearables, cloud computing, wireless communications, automotive, storage and other applications

MIPS M5100



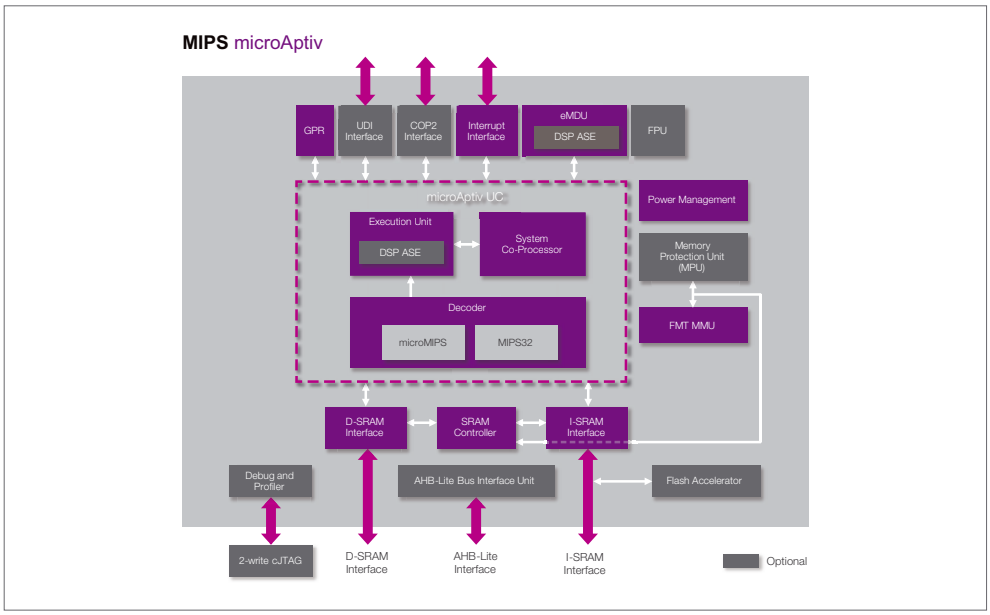
MIPS M5150



Aptiv™ Processor Cores

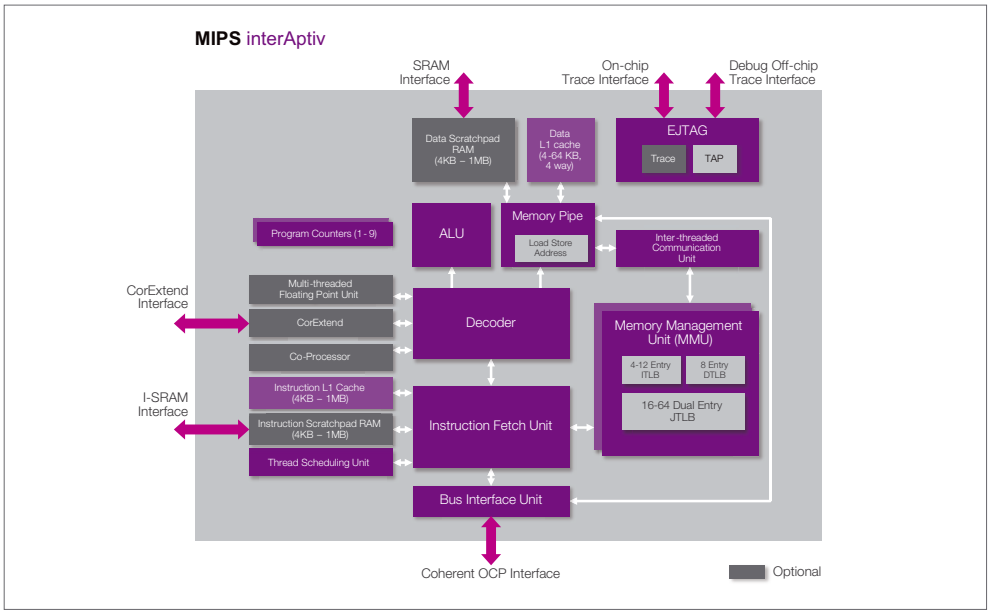
microAptiv™

A highly-efficient, compact, real-time embedded processor core with microMIPS code compression instruction set architecture. Integrates DSP and SIMD functionality to address signal processing requirements for a wide range of microcontroller and entry-level embedded segments including industrial control, smart meters, automotive and wired/wireless communications.



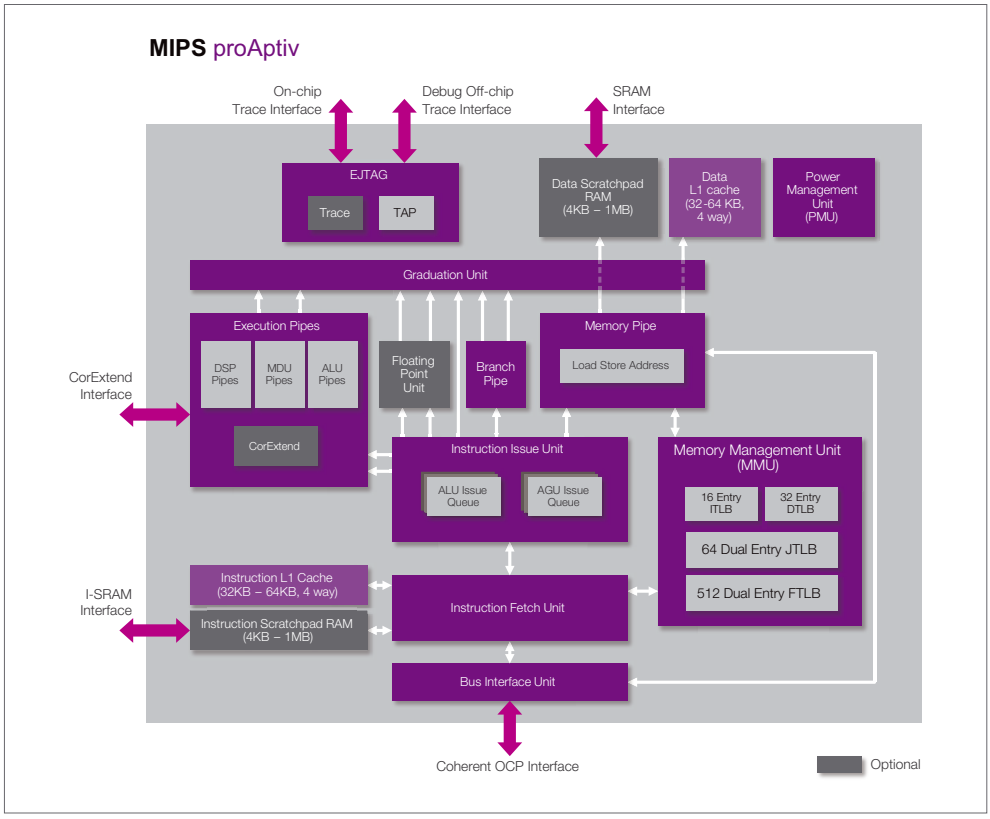
interAptiv™

A multiprocessor core leveraging a balanced nine-stage pipeline with multi-threading to deliver leading performance efficiency. Ideal for highly-parallel applications requiring cost and power optimization, such as smart gateways, baseband processing in LTE user equipment and small cells, SSD controllers and automotive equipment.



proAptiv™

A superscalar, deeply out-of-order processor core that achieves the highest CoreMark/MHz score reported for any licensable IP core, together with leading silicon efficiency. Available in single and multi-core product versions, and ideal for applications processing in connected consumer electronics and control plane processing in networking applications.

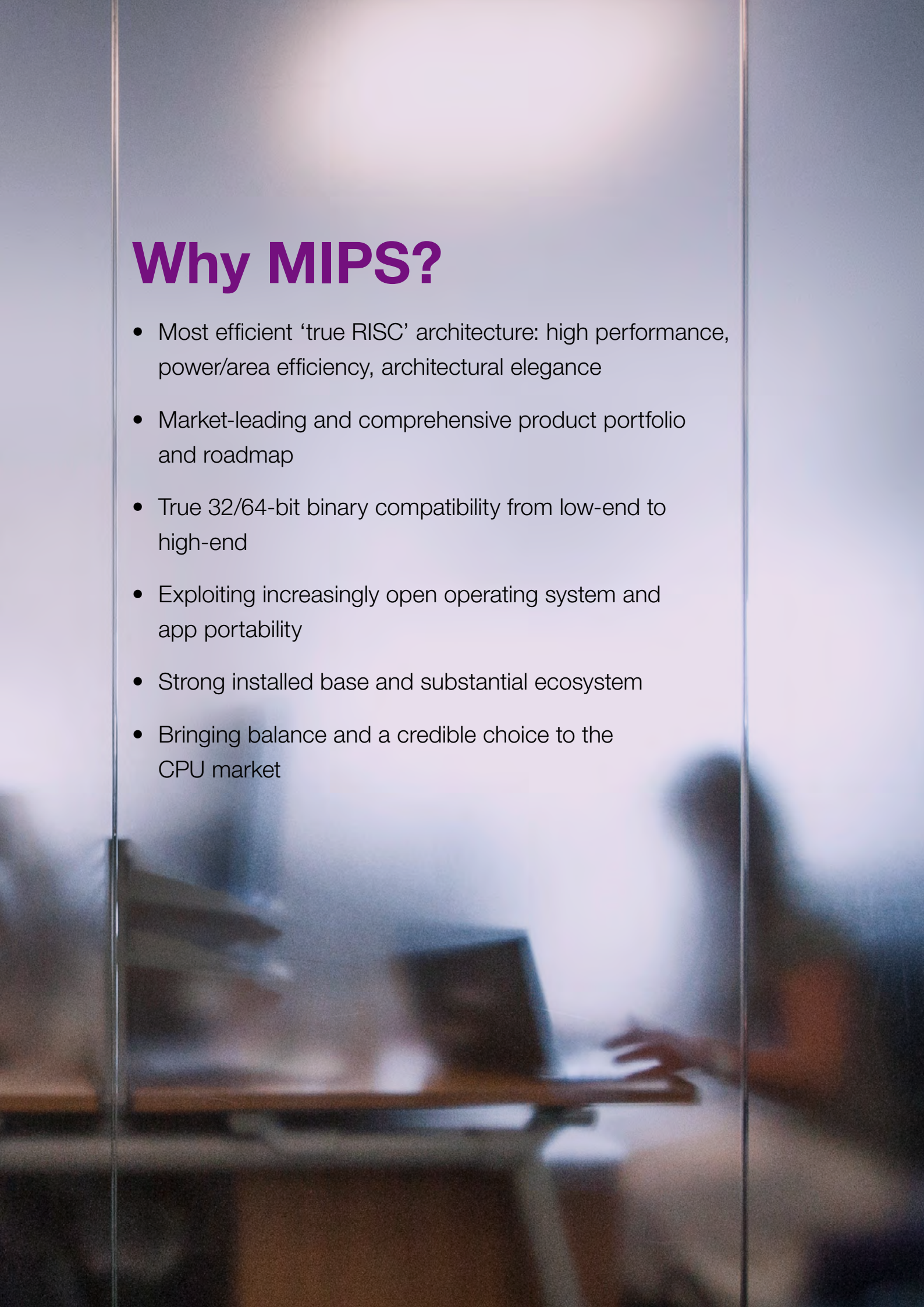


MIPS Tools and Software

Imagination provides a complete portfolio of tools to address all stages of MIPS-based product development. This includes state-of-the-art compiler technology, embedded RTOS and Linux support, EJTAG probes, development boards and more.

Imagination's MIPS toolchain development program is delivering state-of-the-art GCC and proprietary compilers, as well as significant enhancements to Imagination's popular Codescape debuggers, resulting in not only a choice of toolchains to suit every developer environment, but also growing support for heterogeneous debugging.

In addition, with a strong position in home entertainment and networking products and a growing position in mobile devices, MIPS processors power billions of products around the globe, and are supported by a broad ecosystem of software, operating systems and tools.



Why MIPS?

- Most efficient ‘true RISC’ architecture: high performance, power/area efficiency, architectural elegance
- Market-leading and comprehensive product portfolio and roadmap
- True 32/64-bit binary compatibility from low-end to high-end
- Exploiting increasingly open operating system and app portability
- Strong installed base and substantial ecosystem
- Bringing balance and a credible choice to the CPU market

Case Studies

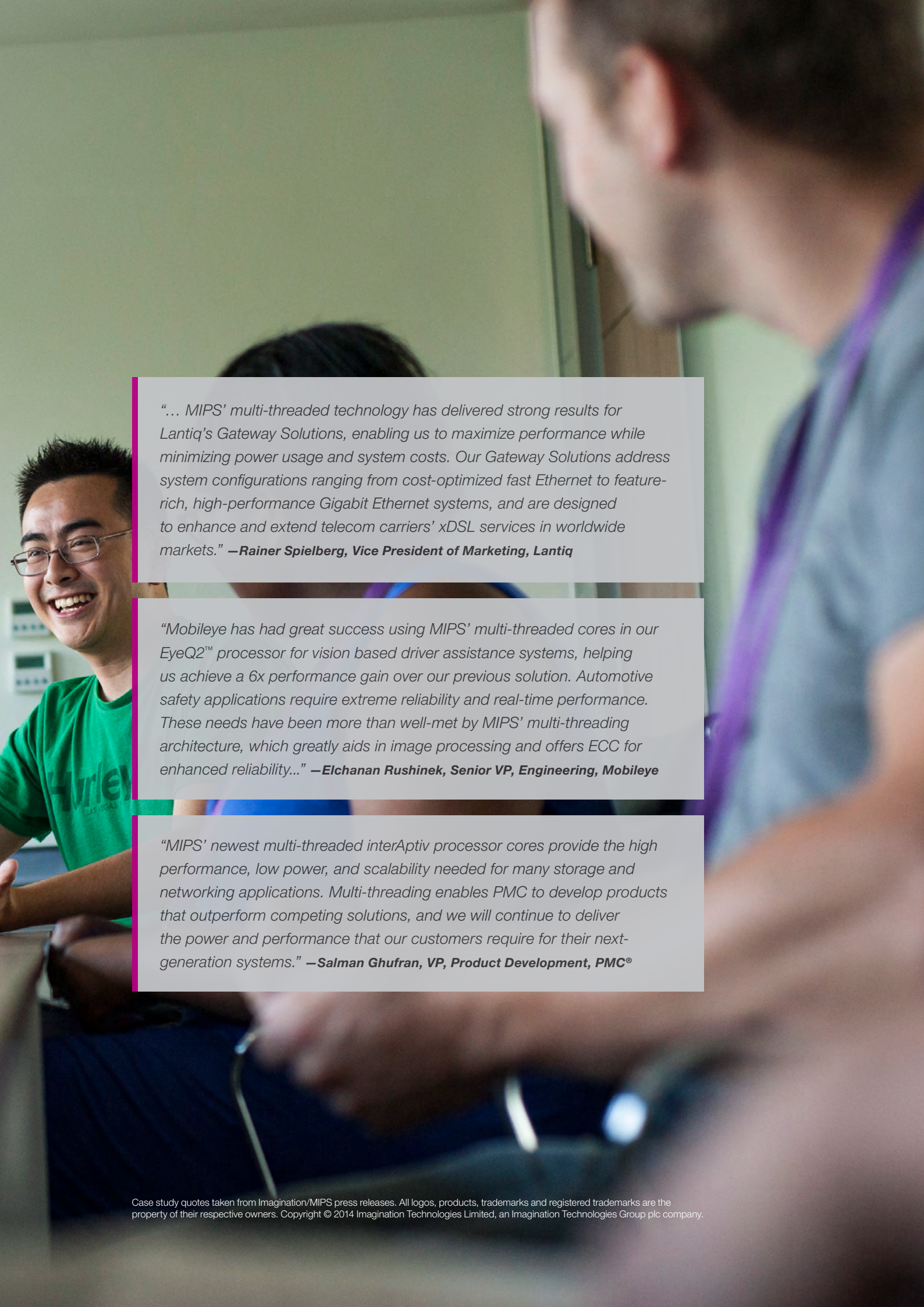
For the past two decades, licensees have been using both the MIPS32 and MIPS64 architectures to create innovative networking infrastructure and consumer electronics products that enhance the way we enjoy digital content.

"As a long-time licensee of the MIPS64 architecture, we are pleased to continue to bring to market new and innovative products based on MIPS, including our new OCTEON Fusion base station-on-a-chip processors, and our next generations of our OCTEON III multi-core processors. The flexibility and scalability of the MIPS architecture along with our architecture license enables us to continue to push the envelope of performance and features of our advanced processors to increasingly higher levels." ***—YJ Kim, General Manager, Infrastructure Processor Group, Cavium, Inc.***

"Microchip Technology's embedded design customers continue to benefit from our successful relationship with MIPS Technologies, via our best-in-class portfolio of 32-bit PIC32 microcontrollers built around the industry-leading MIPS architecture. For microcontrollers, MIPS provides superior performance and more advanced features than the competition..." ***—Sumit Mitra, MCU32 Division Vice President, Microchip Technology Inc.***

"Broadcom is pleased to continue our close working relationship with MIPS to develop the latest flexible, scalable architecture for hardware virtualization, as well as to continue leading the market with highly innovative multicore processors. Our advanced MIPS64-based communications processors combine quad-issue, multithreaded instruction pipelines with up to 128 NXCPU™ processing units for greater performance for enterprise, data center and service provider networks." ***—Ron Jankov, Senior Vice President & General Manager, Processors and Wireless Infrastructure, Broadcom***

"The efficient and scalable MIPS architecture enables us to build processors that are high performance and cost effective, with ultra low power consumption. We are pleased to see continued evolution of the MIPS architecture, with the addition of innovative new instructions that support the next generation of products. In particular, we believe that SIMD functionality will be increasingly important to support media-rich applications in mobile products." ***—Qiang Liu, CEO, Ingenic Semiconductor***



"… MIPS' multi-threaded technology has delivered strong results for Lantiq's Gateway Solutions, enabling us to maximize performance while minimizing power usage and system costs. Our Gateway Solutions address system configurations ranging from cost-optimized fast Ethernet to feature-rich, high-performance Gigabit Ethernet systems, and are designed to enhance and extend telecom carriers' xDSL services in worldwide markets." ***—Rainer Spielberg, Vice President of Marketing, Lantiq***

"Mobileye has had great success using MIPS' multi-threaded cores in our EyeQ2™ processor for vision based driver assistance systems, helping us achieve a 6x performance gain over our previous solution. Automotive safety applications require extreme reliability and real-time performance. These needs have been more than well-met by MIPS' multi-threading architecture, which greatly aids in image processing and offers ECC for enhanced reliability..." ***—Elchanan Rushinek, Senior VP, Engineering, Mobileye***

"MIPS' newest multi-threaded interAptiv processor cores provide the high performance, low power, and scalability needed for many storage and networking applications. Multi-threading enables PMC to develop products that outperform competing solutions, and we will continue to deliver the power and performance that our customers require for their next-generation systems." ***—Salman Ghufran, VP, Product Development, PMC®***

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