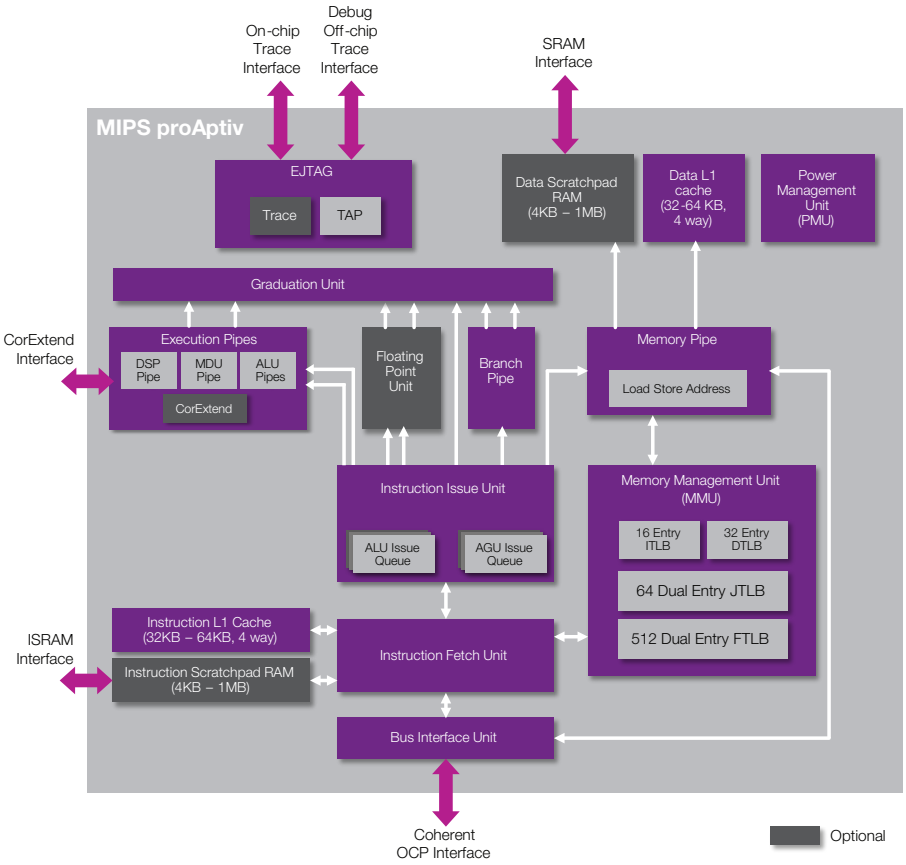
MIPS proAptiv Processor CPU IP Core Family

proAptiv™ processor family is part of the Aptiv™ generation of processor IP cores, designed to deliver the compelling top-line performance required for tomorrow's connected consumer electronics, including smartphones, tablets, connected TVs and set-top boxes.

proAptiv CPUs are based on a multi-issue, deeply out-of-order (OoO) implementation of the MIPS32 architecture, and are available in single and multi-core product versions supporting up to six cores.

The proAptiv family leverages a new base core micro-architecture, a new floating point unit (FPU), and an enhanced multi-core interconnect to deliver a major leap forward in performance over previous MIPS IP cores, while achieving comparable performance at nearly the half the size of competing cores in the same process node.



Features

- 32-bit MIPS32® Release 3 Instruction Set Architecture with up to six cores
- High-performance, 16-stage, multi-issue out-of-order (OoO) pipeline
- I/D L1 cache sizes of 32KB or 64KB each, 4-way set associative
- Programmable Memory Management Unit (MMU)
- MIPS DSP Module, version 2
- Optional 2nd gen hi-performance dual-issue Floating Point Unit (FPU)
- Advanced power management at base core and multi-core cluster levels
- CorExtend™ UDIs, MIPS16e ASE, EJTAG/PDtrace debug

Benefits

- Superscalar, OoO processor available in application-optimized single and multicore versions
- Sophisticated branch prediction for performance on modern software workloads
- Load/Store bonding for optimum data movement performance
- EVA (Enhanced Virtual Addressing) – programmable virtual address map for optimal use of 32-bit address space
- Industry leading benchmark and real world performance without an increase in area and power
- Broad software and ecosystem support and mature toolchain
- Available as synthesizable IP, for implementation in any process node, with standard cells and memories

Applications

- Smartphone/tablet
- Connected DTV/STB
- Networking
- Automotive infotainment

High-performance, 16-stage, out-of-order (OoO) pipeline

- Quad instruction fetch, triple bonded dispatch per cycle
- Instruction peak issue: 4 integer + 2 FPU operations/cycle
- Sophisticated branch prediction, plus L0/L1/L2 branch target buffers, return prediction stack, jump register cache
- Instruction bonding – merges two adjacent 32-bit accesses into one 64-bit access for 2x increase on data movement ops
- UnCached Accelerated (UCA) writes – for high performance bulk data transfers to GPUs and other on-chip peripherals

Programmable Memory Management Unit (MMU)

- Enhanced Virtual Address (EVA) provides better utilization of 32-bit address space
- 1st level micro TLBs (uTLBs) – 16 entry iTLB, 32 entry dTLB
- 2nd level TLBs – simultaneous access, var/fixed page sizes
  - 64x2 entry VTLB, 512x2 entry 4-way set assoc. FTLB

MIPS DSP Application Specific Extension (ASE), version 2

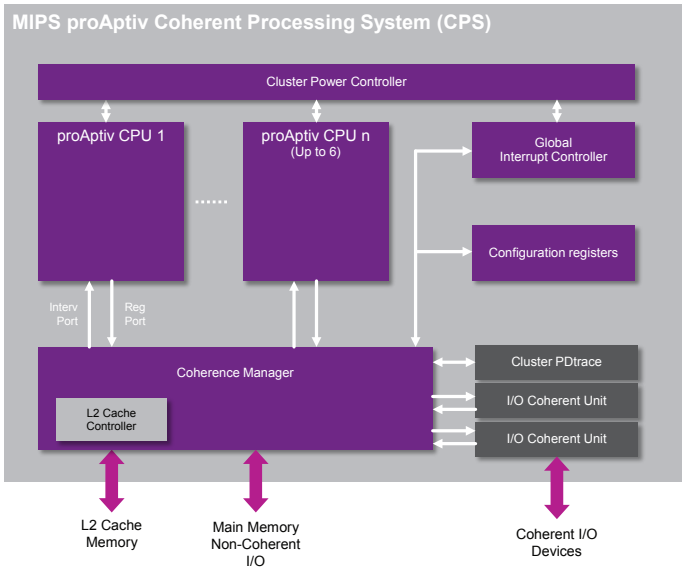
- 4 accumulator reg. pairs, fractional d-types, saturating math
- SIMD instructions operate on 2x16b or 4x8b

2nd gen high-performance dual-issue Floating Point Unit (FPU)

- IEEE-754 compliant
- Full speed with CPU

Coherent Multi-Core System

- Product versions supporting 1 up to 6 cores
- Second generation enhanced Coherence Manager (CM) with 256-bit wide internal datapaths and integrated L2 cache controller with programmable wait states
- Multi-core level IP blocks for global interrupts (GIC), cluster power control (CPC), configuration registers (GCRs), program/data tracing (PDtrace), and hardware accelerated I/O coherence (IOCU)



Power Management Features

- Multi-core cluster power controller (CPC)
  - Per CPU voltage domain gating; per CPU clock gating
  - Cluster level DVFS capable
- Core level
  - Coarse and fine-grained clock gating
  - Way prediction on data and instruction L1 caches
  - Instruction and register-based sleep modes

Development Tools, Software and Ecosystem Support

- Open source tools and operating systems
  - MIPS optimized Android, Linux, and GCC
- MIPS Navigator™ Integrated Component Suite (Nav ICS)
  - Eclipse based IDE
  - Compiler/debugger - Sourcery Codebench from Mentor
  - MIPS IASim™ instruction accurate simulators
- MIPS hardware
  - Malta hardware evaluation platform and debug probes
- Extensive leverage of other existing MIPS32 third party ecosystem solutions for tools, OS, RTOS, compilers, simulators etc.

Baseline Specifications

Target Specifications	TSMC 28HPM
Frequency	1 GHz - 2+ GHz*
CoreMark/MHz (per core)	5.1
Total CoreMark @ 1.5 GHz	> 7500 per core
DMIPS/MHz (per core)	3.5
Total DMIPS @ 1.5 GHz	> 5250 per core

Notes: Frequencies indicated are for fully floorplanned dual core implementation, ranging from 12T SVt area-optimized in worst case silicon corner, to 12T MVt speed-optimized typical corner silicon.

Each base core configuration:

- 32KB Data/Inst L1 caches with parity, BIST
- New high-speed FPU
- Fully-featured MMU, using multi-level TLB (I/D uTLBs + 128 entry VTLB + 1024 entry FTLB)
- PDtrace™ debug

Multi-core cluster configuration:

- Dual fully-configured proAptiv cores per above
- Coherence Manager + integrated 1MB L2$ w/ECC
- One hardware IO Coherence Unit (IOCU) port
- Cluster level PDtrace

Implementation libraries/parameters – speed optimized, based on:

- TSMC 28HPM 12T standard cells + Synopsys memories
- Worst case, slow-slow corner silicon (zero temp, WCZ) with 10% OCV + 25ps clock jitter margins, except where noted at typical silicon.