*[**TUTORIAL]** MIPSfpga: Using an Industrial Non-Obfuscated MIPS Soft-Core on an FPGA for Education*

‘Hands-on with a non-obfuscated MIPS core for teaching and projects!’

Using the Digilent Nexys 4 DDR platform with a Xilinx Artix 7 FPGA

7th September 2017 FPL 2017, Ghent, Belgium

The Imagination University Programme is pleased to host a tutorial specifically for teachers, based on the award winning “MIPSfpga” teaching materials. The latest version of these materials called MIPSfpga v2 reflect the maturity of materials now licensed by more than 500 universities globally, and now includes 25 in-depth exercises which take students both around the core configuring peripherals, and then go inside to look at cache memory and pipeline operation. There has never been a better way to give your students genuine insight into the state-of-the-art in RISC processors. We remind you that MIPSfpga provides the RTL source code of the MIPS microAptiv for implementation on an FPGA. It is a member of the same family found in many embedded devices, including the popular PIC32MZ and PIC32MK microcontrollers from Microchip. It’s a current and successful IP core.
This tutorial will show you how to use this core as part of a Computer Architecture course, which will pave the way for your students to use it in their projects, creating their own SoC designs. MIPSfpga is the real “industrial” RTL, non-obfuscated, and available freely for academic use. This tutorial is the start of a global programme of events to enable teachers to harness this wonderful technology. At FPL, you can be the first to get hands-on with MIPSfpga v2!

Location: Room TBC Culture and Convention Centre Het Pand, Ghent, Belgium

Date: **7th September 2017**

Agenda **The MIPSfpga 2.0 workshop will cover four main areas:**

1. Overview & use of the MIPSfpga system and core
2. Performance counters & interrupts
3. MIPSfpga (uAptiv) core & adding instructions
4. Memory systems

An overview of the schedule is as follows:

- Introduction to MIPSfpga
    - Setting up a Vivado Project for MIPSfpga
    - Programming and debugging on MIPSfpga
- Modifying MIPSfpga, I/O & measuring performance
    - Adding peripherals (7-segment displays, light sensors, etc.)
    - Using interrupts for I/O
    - Using uAptiv's performance counters
- Introduction to the Imagination University Programme
- Understanding & modifying the uAptiv core
    - Core overview & organization
    - Tracing instructions through the pipeline
    - Adding instructions using CorExtend
- Exploring & modifying the MIPfpga memory system
    - Exploring cache configurations, write policies, and optimization techniques
    - Adding a scratchpad RAM
- MIPSfpga SoC
    - Hands-on guidance to set up MIPSfpga as a system on a chip running Linux

After your full day of training you will be proficient in using MIPSfpga v2 and be aware of its potential to revolutionise your teaching of Computer Architecture.

All delegates will be given access to:

- **MIPSfpga core**
- **The full Getting Started Guide** (written by Prof. Sarah Harris, co-author of Digital Design & Computer Architecture by Harris & Harris, with contributions from Xilinx)
- **Detailed reference documentation** about MIPS microAptiv.
- Other vital information/programs that enable the whole package to work effectively.

Trainers

• Professor Daniel Chaver-Martinez	University de Complutense, Madrid
• Zubair Lutfullah Kakakhel	Software Engineer, Imagination Technologies
• Robert Owen	Manager, Imagination University Programme

Eligibility

- Free to all FPL convention participants who are registered our MIPSfpga tutorial.
- Priority will be given to academics involved directly in teaching.
- The tutorial will be given in English
- Prior experience of Vivado or Codescape MIPS SDK is useful but not essential.
- If over-booked, we reserve the right to accept or refuse registrations based on our desire to enable the widest number of universities and colleges to participate.

Meet the "IUP" Imagination University Program

- Meet us at the Imagination University Programme Booth
  Date and Time: **TBC**

Registration Please apply online here
Note: Interested parties will have to be registered for FPL 2017 conference, in order to participate in our tutorial. Please register at https://www.fpl2017.org/registration.

Find out about the Imagination University Programme
We would appreciate it if you can circulate this e-mail to academic friends and colleagues…

Best Regards,

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