EJTAG Implementation Application Note

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1 Introduction

This document should be read together with the EJTAG specification (Reference [1]). It is intended as a practical guide to implementors of both target systems and probes, to assist in achieving the maximum possible performance in terms of speed and reliability over the JTAG serial link.

This document does not form part of the EJTAG specification and does not update or change this specification in any way. The information given is considered to be useful in ensuring that probe and target systems that implement EJTAG perform as well as possible, and are as interoperable as possible.

2 Timing

The timings from the EJTAG specification are reproduced in Figure 1 and Table 1.

First, it should be noted that the critical timings are all concerned with the negative half-cycle of the TCK clock. Therefore, for maximum speed, a probe should run with the positive halfcycle of the TCK clock as short as possible, i.e. 10ns.

Figure 1 Test Access Port Signals Timing

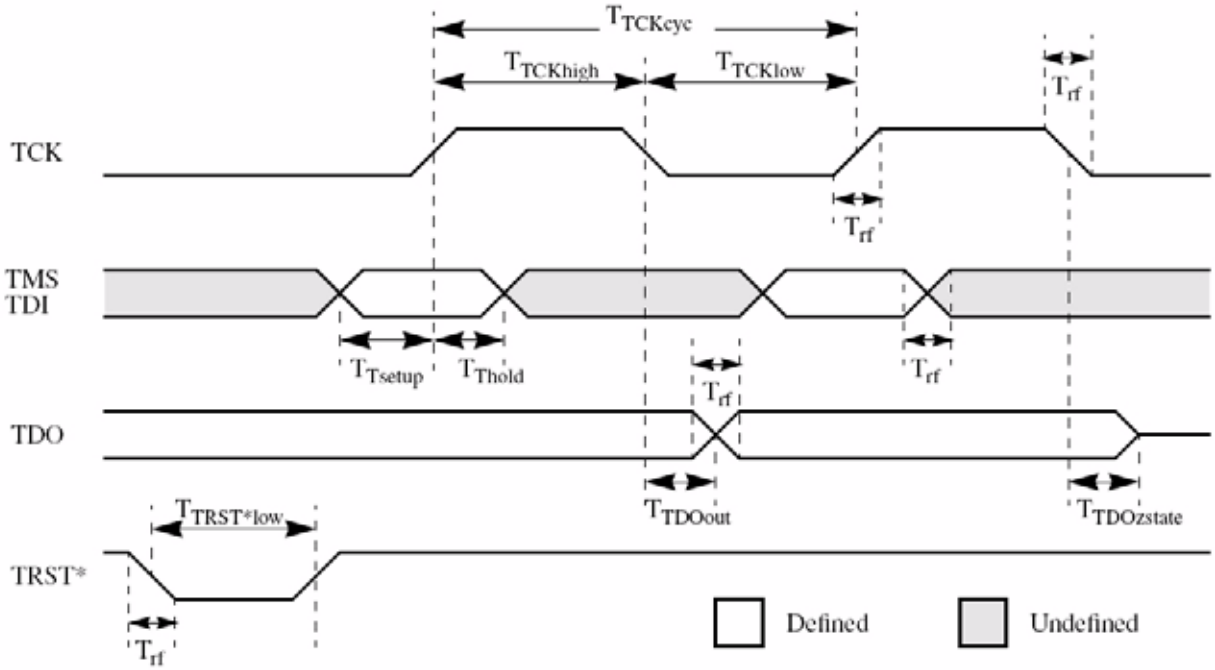


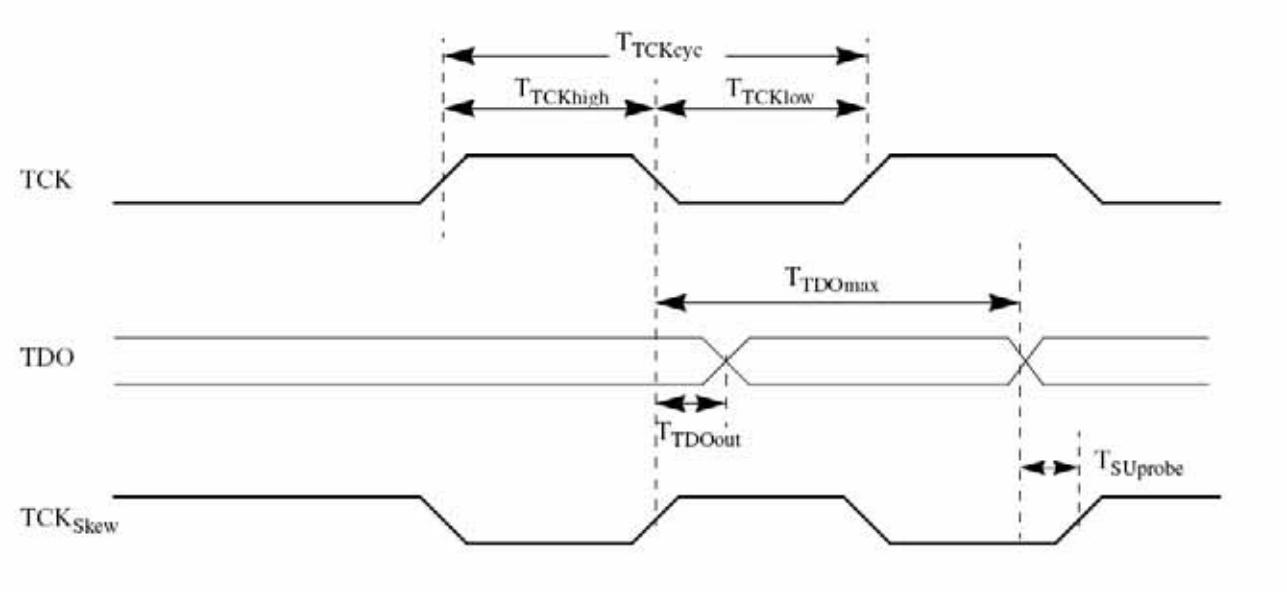
Table 1 Test Access Port Signals Timing Values

Symbol	Description	Min	Max	Unit
T_{TCKcyc}	TCK cycle time	25		ns
$T_{TCKhigh}$	TCK high time	10		ns
T_{TCKlow}	TCK low time	10		ns
T_{Tsetup}	TAP signals setup time before rising TCK	5		ns
T_{Thold}	TAP signals hold time after rising TCK	3		ns
T_{TDOout}	TDO output delay time from falling TCK		5	ns
$T_{TDOzstate}$	TDO 3-state delay time from falling TCK		5	
$T_{TRST*low}$	TRST* low time	25		
T_{rf}	TAP signals rise / fall time, all input and output		3	

Secondly, The limiting timing parameters in a real system are likely to be the target system's T_{TDOout} plus the probe's input setup time (typically relative to TCK rising edge), which together limit the minimum TCK low period. A real target system, where there may be some distance from the CPU device to the probe connector (which may be close to the board edge for practical reasons), may have trouble meeting the maximum 5ns specified for T_{TDOout}.

These limitations can be minimized by skewing the clock which is used to register TDO in the probe from the actual TCK. See signal TCK_{Skew} in Figure 2 as an example - note that the timings are shown at the probe, i.e assume zero probe cable delay. This clock can be made later than TCK - its rising edge can be generated when the probe outputs its TCK *falling* edge, without risk of violating any timing. Thus the allowable T_{TDOout} in the target system can be up to T_{TDOmax} as shown in Figure 2.

Figure 2 TDO Timing at Probe with Skewed Probe Sample Clock



Using the above techniques, an optimal system could have a TCK high time of 10ns, a TCK low time of 15ns, and the allowable delay in the target system could be up to 25ns (less probe setup time) before this would limit the 40MHz maximum clock rate.

This skewing can also incorporate any known delay in the probe-target cable, so cabling can be made reasonably long, as long as the length is known, without giving a speed penalty.

3 Signal Quality

The most significant barriers to good signal quality in EJTAG target connections appear to be impedance matching, capacitive loading, and noise/crosstalk.

3.1 Impedance Matching

Typical impedance values for the PCB traces are generally between 50 and 100 ohms. Unshielded ribbon cable, with a “ground, signal, ground” distribution tends to have an impedance around 100 ohms, although if it is shielded this will drop to around 50 ohms.

To ensure that impedance mismatches do not cause excessive signal edge degradation (particularly on the TCK signal) it is therefore recommended that the probe series terminates the signals it drives with an effective impedance of 75 ohms (buffer output impedance plus external resistor).

For TDO, the value of external resistor recommended in the EJTAG Specification (33 ohms) when added to the likely output impedance of a typical buffer on an ASIC, should also give a match that it good enough. TDO is also less critical as it is not edge-sensitive.

3.2 ESD Protection and Capacitive Loading

As the EJTAG signals will typically go directly between the “outside world”, with risks of static discharge and over-voltages, and a highly integrated device which may be sensitive to these conditions, it is advisable for target systems to implement overvoltage protection devices on all the EJTAG signal lines.

Some of these devices can have a very high loading capacitance, which can significantly slow the EJTAG signals, so it is recommended that devices with a capacitance of 35pF or under are used. A suitable device is the SN65520 from Texas Instruments.

3.3 Noise

As recommended in the EJTAG Specification, 1k pull-up resistors should be added to the EJTAG signals on the target board, which will not have any terminating effect but should reduce susceptibility to noise, and guarantee signal levels in the case that the probe is not driving.

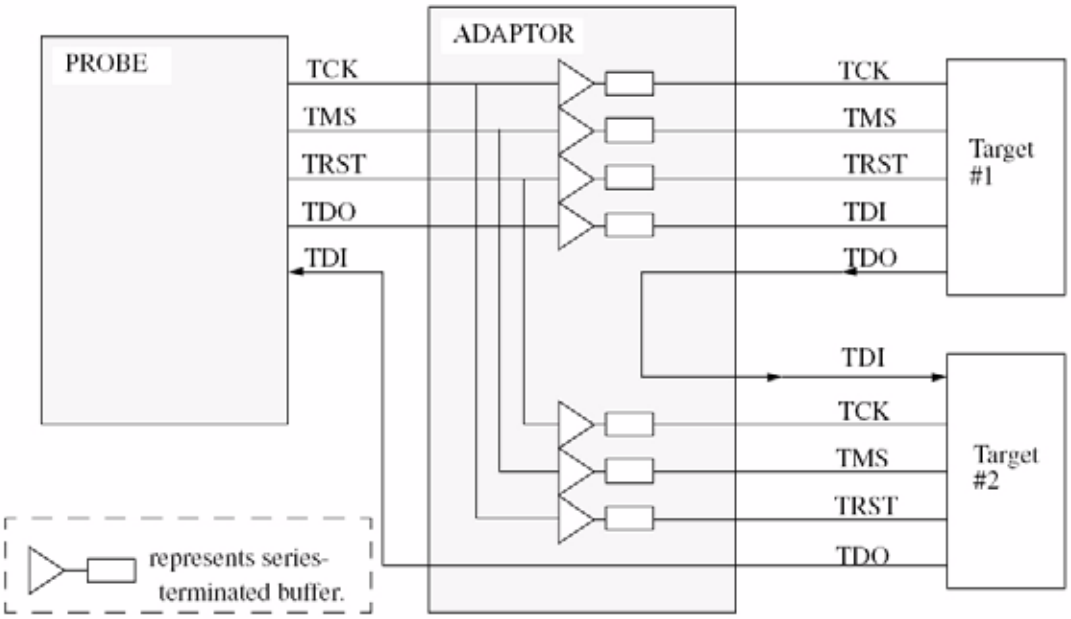
If the ribbon cable is long, then shielded ribbon cable could be considered as an option.

4 Multi-drop

For systems with multiple CPUs which are not on the same target board, it may be necessary to daisy-chain the EJTAG cable between multiple target systems.

For this to work effectively, signals which are common to the systems and driven by the probe, i.e. TRST, TCK, TMS should be buffered individually to each target system. This is illustrated in Figure 3, which shows an adaptor fitted to the probe. Note that the adaptor is fitted “close” to the probe, i.e. the longest wires are those from the adaptor to the target systems.

Figure 3 Multi-drop Configuration



It should not be necessary to buffer the TDO/TDI signals between the boards, unless the cables are long, and/or the boards present a high capacitive load which will slow the signal excessively.

5 References

1. EJTAG Specification
MIPS Document: MD00047

5 References