An Introduction to the MIPS32® M14K™ Processor Core

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1 Introduction

MIPS Technologies, Inc. is a provider of synthesizable, licensable 32-bit processor cores offered with a range of features and capabilities that address diverse market segments including home entertainment (e.g. DTV and set-top boxes), home networking (e.g. xDSL and WiFi), personal entertainment (e.g. digital cameras and portable media players) and microcontrollers (MCUs). MIPS also licenses its 32- and 64-bit architectures to system-on-chip (SoC) developers.

The MIPS32® family of processors is based on a standard, compatible architecture. MIPS32 4K®-based processor cores including the MIPS32 M4K®, 4KE® and 4KSd™ cores are specifically designed to address the requirements of high performance, low power and ease of design for cost-sensitive embedded applications such as MCUs and consumer electronics.

A superset of the M4K core, the MIPS32 M14K core is one of the newest members of the 4K family, and one of the first MIPS® processors that includes the microMIPS™ code compression Instruction Set Architecture (ISA). microMIPS offers MIPS32 performance with equivalent 16-bit code density. The M14K core incorporates design enhancements and application-specific features that are optimized for flash-based MCU and real-time embedded control applications.

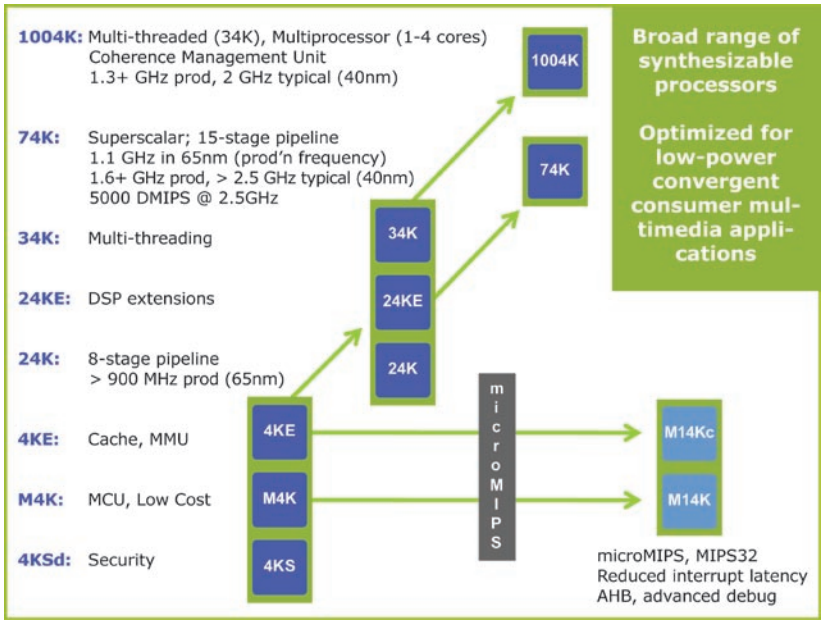

Figure 1: MIPS32 processor core roadmap

1.1 Performance Efficiency

Achieving higher levels of performance is not only a function of increasing the clock frequency, but is also influenced by the instruction per cycle (IPC) efficiency of the execution unit, the depth of the pipeline core and the speed of access to memory-resident code and data.

Performance efficiency is a combination of operating clock frequency and IPC that provides a practical measure of the optimal frequency, power and silicon size a device will use in executing a specific application.
The M14K core is based on the established 4K microarchitecture that delivers high performance efficiency from a 1.5 DMIPS/MHz execution unit. The M14K core can achieve a production frequency of 180 MHz in a 130nm standard process.

1.2 Cost Reduction

Minimizing silicon cost without compromising performance or software development capabilities is a key design criteria and competitive differentiator for MCU developers.

The M14Kc core implements the new microMIPS ISA that can reduce code memory size by 35% compared to MIPS32—leading to a corresponding reduction in silicon size and cost.

A high level of configurability and build-time options designed into the architecture lead to additional cost savings. The synthesizable, scalable M14Kc processor core maintains a high level of performance at lower clock frequencies across a wide range of geometries and standard processes, enabling an additional reduction in silicon size by synthesizing to a smaller, area-optimized configuration.

1.3 Application-Specific Features

A unique combination of intensive signal processing, deterministic operation and a wide range of I/O connectivity attributes typically found in control-type applications define and determine the type of features and functions that are required for an effective MCU solution.

Microcontroller-centric systems, such as those found in the industrial control, automotive and consumer markets, are being designed with an increasing number of interrupts and higher clock frequencies, yet have more stringent real-time requirements. The M14K core addresses this with enhanced interrupt handling capabilities to reduce interrupt latency, as well as hardware multiply/divide unit and atomic-bit instructions that accelerate task completion in the reduced timeframe available.

The majority of MCUs integrate two types of memory on-chip or close to the processor core. Small amounts of SRAM provide the storage for data, with a much larger size flash memory containing the program code and fixed data storage. Flash access speeds are an

order of magnitude slower than the operating frequency of the processor, introducing execution delays that considerably reduce instructions per cycle (IPC). The M14K core adds special pre-fetch buffer circuitry to obviate the slowness of the flash memory, thereby improving access speed and performance efficiency.

A new feature in the M14K core is the introduction of an optional AHB-Lite Bus Interface Unit (BIU), which enables standard connectivity to a wide range of I/O peripherals commonly used in MCU applications.

1.4 Fast Time-to-Market

Microcontrollers, especially 32-bit MCUs, are becoming increasing more complex subsystems incorporating more advanced features and running more complex software. This makes product debug and development critical in overall project management, and key in determining time to market.

The M14K core has an easy-to-program and well-established architecture, supported by a large set of hardware and software development tools that are available from MIPS Technologies and a range of third party vendors.

The M14K core includes several on-chip debug and profiling features, available through the industry-standard EJTAG port, that enable faster, and more accurate, hardware and software by efficient use of iFlowtrace™, breakpoints, data address sampling, performance counters on multiple event types and 'hot-spot' analysis. All of these are supported within the MIPS System Navigator™ debug probe.

The MIPS-supplied SoC development platform SEAD-3 and a set of cycle accurate and instruction accurate simulators provide additional reductions in development time and cost. These technologies enable designers to develop hardware and software in parallel with a comprehensive and flexible co-simulation environment.

1.5 Expandability

The M14K core supports connection to microcontroller-specific peripherals through the standard AMBA AHB-Lite bus interface.

The M14K core includes the optional support of Co-Processor2 (CoP2) and CorExtend™ expansion features that are available across the range of MIPS processor cores. The CoP2 interface enables high performance communication with the M14K core and customer-specific IP. The CorExtend User Defined Interface (UDI) block enables the implementation of application-specific instructions to be tightly coupled to the processor, extending the capabilities of an M14K-based microcontroller system design.

2. M14K Processor Architecture and Features

At the heart of the M14K core is a 5-stage pipeline load/store execution unit that is MIPS32 Release 2 Architecture compliant, delivering a Dhrystone performance of 1.5 DMIPS/MHz.

The central core is a dual-decoder design incorporating the industry-standard MIPS32 instruction decoder and the microMIPS ISA decoder, providing both legacy MIPS32 code support and advanced code compression capability.

The M14K is a superset of the M4K processor core, designed from the same 4K micro-architecture, with additional features including enhanced interrupt handling, reduced interrupt latency, additional debug/profiling modes, native AHB-Lite Bus Interface Unit and a reference design to accelerate flash memory access.

Connection to memory is via a simple SRAM-style interface, configurable in either unified or dual instruction/data interfaces. The M14K core contains required and build-time optional functional blocks with a high degree of configurability, allowing the design to be more closely aligned with the requirements of the system design.

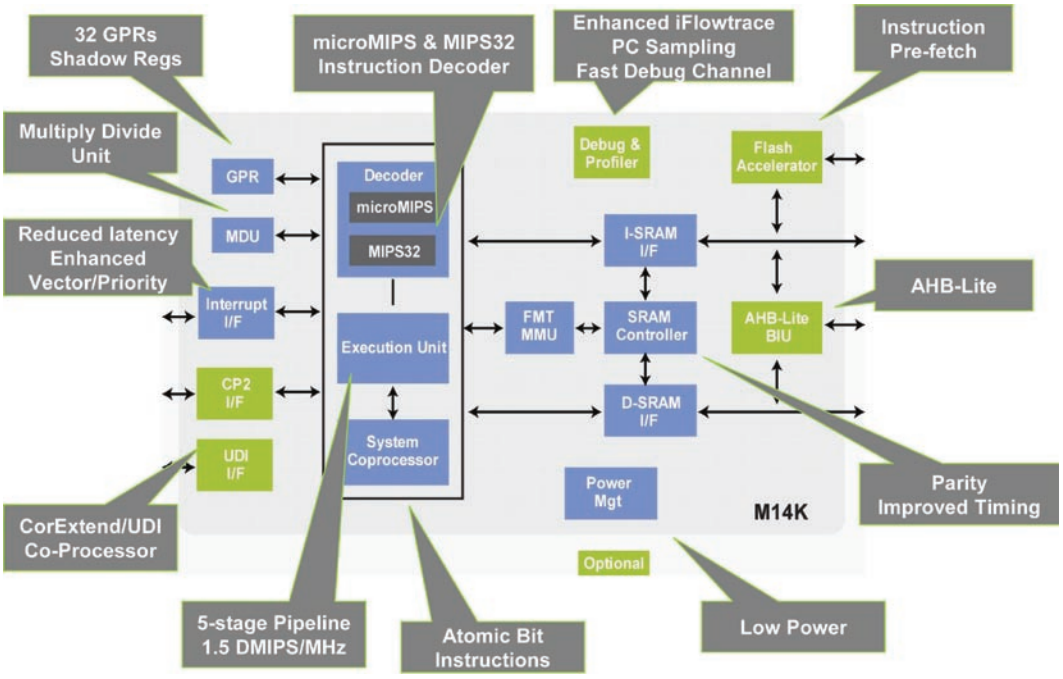

Figure 2: M14K core feature block diagram

2.1 Retained Features from the M4K Core

The M14K core retains all of the basic features from its predecessor, the M4K core, including the MIPS32 instruction set compute engine, shadow register sets, vectored interrupt controller, multiply/divide unit (MDU), memory management unit (MMU), and SRAM controller. The M14K core maintains full backward-compatibility with the MIPS32 architecture, as well as the 4K core pipeline flow and functionality.

The M14K core pipeline has 5 stages (see fig 3), with a bypass mechanism that allows the result of an operation to be sent directly to the instruction that needs it without having to perform the register write-read operation, reducing latency and improving IPC. microMIPS instructions are recoded during the I-stage.

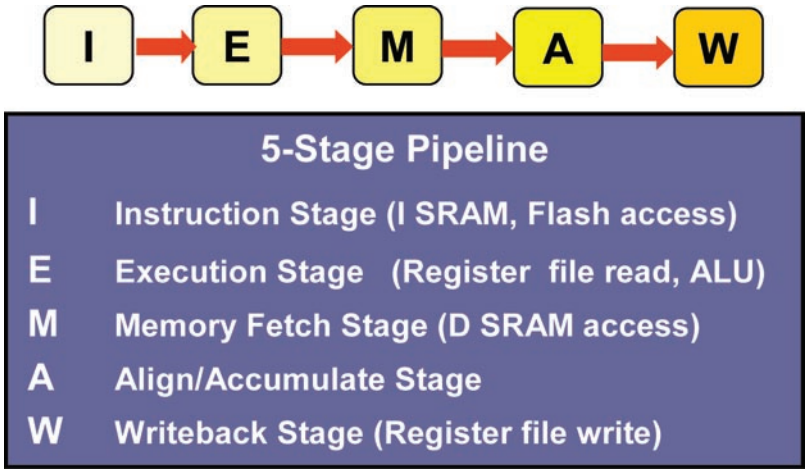

Figure 3: 5-stage pipeline

The M14K core contains thirty two 32-bit general purpose registers (GPRs) used for address calculation and integer data manipulation. Additional 32-bit register files, up to 16 sets, are optionally available for use as shadow registers to improve the latency and context switching of interrupt handling routines.

The MDU has its own pipeline that operates in parallel with the core pipeline, which does not cause long operations, such as divide, to stall execution of other system code. The MDU supports execution of 16x16 and 32x16 multiply operations every clock cycle, and 32x32 in 2 clock cycles. 32-bit divide operations complete in 33 cycles. The MDU supports MAC-type instructions commonly used in DSP applications.

The M14K core contains a Fixed Mapping Translation (FMT) MMU that provides a virtual-to-physical address translation with selectable attributes, interface between the Execution Unit and SRAM controller.

The SRAM controller provides a high-performance, configurable interface to tightly coupled SRAM-type memories and to the optional flash accelerator and AHB-Lite BIU. The SRAM interface includes separate uni-directional 32-bit wide buses for address, read and write data, with a build time option to select either dual or unified instruction and data interfaces. The SRAM controller has advanced control features such as Back

Stalling, allowing connection to slower devices, and Transaction Abort, allowing long execution cycles to be aborted. This is particularly useful in reducing latency when interrupts are pending. The controller also generates separate byte enables that enable connection to memories of less than 32-bits wide.

2.2 microMIPS ISA

The M14K core is one of the first MIPS processors designed with the microMIPS code compression ISA included in the core design. microMIPS is a complete ISA with a mix of both 16- and 32-bit instructions that supports all MIPS32 instructions, with some of the most commonly used instructions recoded into 16-bit instructions. microMIPS includes 15 new 32-bit instructions and 39 new 16-bit instructions. microMIPS delivers 98% of MIPS32 performance while reducing memory size by 35% versus code containing MIPS32-only instructions.

Figure 4 shows the results of relative Dhrystone performance and code size reduction executing the CSiBE benchmark for MIPS32 and microMIPS.

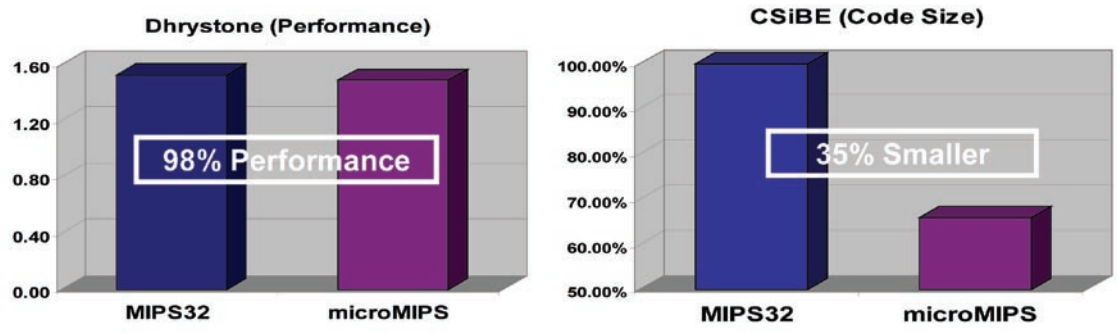

Figure 4: microMIPS performance and code size

The microMIPS instruction decoder fits inside the existing 4K pipeline architecture without affecting compatibility with the microarchitecture. Logic has been implemented to support and control misaligned instructions, improving performance and code density. microMIPS supports co-existence with the legacy MIPS32 decoder, and is assembly level- and ABI-compatible with MIPS32.

Support for microMIPS code development and debug is provided by a complete software toolchain and hardware development platform.

2.3 Interrupt handling

Typical microcontroller systems have a high number of interrupts, with the majority connected to critical real-time functions that require efficient servicing in a constrained number of clock cycles to enter into and implement the Interrupt Service Routine (ISR).

The M14K core has several advanced features in the interrupt handling mechanism that extend the number of serviceable interrupts to 255 from an external controller, and enhanced hardware assist to reduce the vector generation and context switching times.

The M14K implements a new hardware-assisted feature, combined with the use of shadow registers, that reduces interrupt latency (the time from when the interrupt is recognized to the start of ISR execution). This is accomplished through the use of faster interrupt vector prefetching and dedicated hardware to automatically read and store the core status and GPRs. A similar mechanism is used to unwind the stack and restore the core state when exiting the interrupt service. Interrupt latency is 10 cycles to enter the service routine (Interrupt Prologue) and 4 cycles to exit from the service routine (Interrupt Epilogue).

The M14K also implements interrupt chaining, reducing the time needed to service multiple valid interrupts that may be pending at the same time. A new instruction (IRET), with the use of dedicated hardware including shadow registers, automates the Interrupt Epilogue and tailchaining process, reducing latency to 4 and 7 cycles respectively.

2.4 Flash Access Acceleration

The M14K core includes a reference design that accelerates access to slow flash memories that contain the operating code, and typically the RTOS and application software. The circuit is based around a pre-fetch buffer design with a configurable data bus width up to 128-bits, providing a small cache for flash data.

The design is supplied in a default configuration of two 128-bit line entries with each line having an associated Tag and 4 valid-word bits that are used in the process of determining if the required instruction is in the pre-fetch buffer. This can be modified and configured by the SoC designer to fit the specific design requirement.

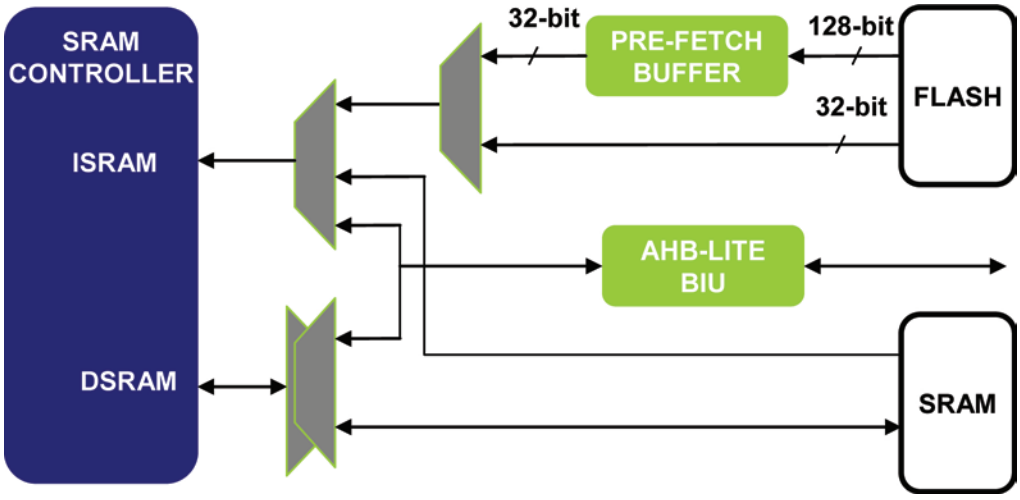

Figure 5: Flash accelerator and AHB reference design

To illustrate how much this flash access accelerator design can improve the Cycle per Instruction (CPI) capability of the M14K core, consider the following example:

Assume –
M14K core operating at 100 MHz, and flash memory access of 50ns (20 MHz)
A typical code sequence comprised of 8 instruction fetch and 2 load/store operations.

- Flash access = 5 clocks
- SRAM/Pre-fetch buffer access = 1 clock

CPI with no pre-fetch circuitry would be:
((8x5) + (2x1))/10 = **4.2**
CPI with pre-fetch circuitry would be:
100% hit rate = ((8x1) + (2x1))/10 = **1.0**
50% hit rate = ((4x1) + (4x5) + (2x1))/10 = **2.6**

Implementing the pre-fetch acceleration circuit in this example could achieve a 4x CPI improvement.

2.5 Debug and Profiling

An Enhanced JTAG (EJTAG) interface provides the physical access for high-speed debugging and profiling of an M14K-based system. The EJTAG interface connects to the Test Access Port (TAP) used for transferring trace and debugs data between the M14K core and debug probe.

The M14K core provides both simple and complex breakpoint support, configurable to a wide range of instruction and data breakpoint types. Instruction/data breakpoint and iFlowtrace debug capabilities are retained from the M4K with Fast Debug Channel (FDC), Performance Counters (PCs) and PC data/address sampling functions added to enrich the debug and profiling capabilities.

iFlowtrace is a low-cost, efficient facility that traces the instruction PC. The M14K core adds special event and tracing modes to iFlowtrace, extending its usability and effectiveness in accelerating system debug and development. For program analysis, two new sets of Performance Counters can be used to count internal, predefined events, such the number of specific instructions that have been executed in a set time period. Instruction PC and/or load-store addresses can be sampled periodically to provide data for use in ‘hot-spot’ analysis and program profiling.

The M14K core contains an optional Fast Debug Channel (FDC) that provides high bandwidth access to the M14K core status with low overhead and interruption to the processor core—in effect, offering a real-time debug capability.

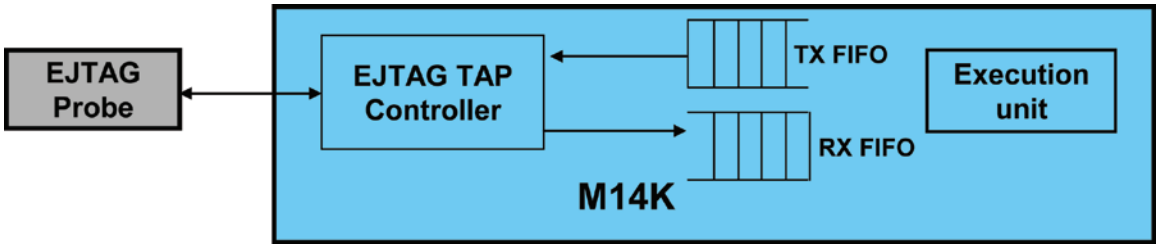

Figure 6: Fast Debug Channel

The FDC incorporates two configurable FIFOs to buffer receive and transmit data that is transferred serially between the debug probe and M14K control logic.

2.6 Configurability

With the M14K core, designers can enable or configure a significant number of features at either build time or during run-time, allowing for implementation of an optimized, cost-minimized specific application. Table 1 summarizes the configuration options available.

Feature	Configurability
microMIPS	optional
Shadow register sets	1,2, 4, 8 or 16
MDU	Speed- or area-optimized
AHB-Lite	optional
Flash accelerator	optional
SRAM interface type	separate or unified I/D
Parity support	optional
Interrupt vector generation	vector input or 16-bit register
EJTAG	optional
iFlowtrace 2.0	optional
PC sampling	optional
Performance counters	optional
Instruction/Data breakpoints	0/0, 2/1, 4/2, 6/2, 8/4
FDC FIFO	2 Tx/2 Rx, 8 Tx/4 Rx
Power management	clock gating, WAIT instruction
CoProcessor 2	optional
CorExtend/UDI	optional

Table 1: Configurability options

3.0 Summary

The M14K is one of the first MIPS processors designed with the new microMIPS ISA, resulting in an enhanced high-performance, low area/cost, and low-power MIPS32-compatble core successor to the M4K core.

The M14K core is supported by a comprehensive, integrated set of software and hardware development tools, a new evaluation/development platform and a broad ecosystem of third party partners.

With a high-performance and efficient 1.5DMIPS/MHz microarchitecture and advanced code compression capability from microMIPS, along with new and enhanced application-specific features, the M14K core an ideal solution for microcontroller and real-time embedded system design.