An Introduction to the MIPS32® M14Kc™ Processor Core

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1 Introduction

MIPS Technologies, Inc. is a provider of synthesizable, licensable 32-bit processor cores offered with a range of features and capabilities that address diverse market segments including home entertainment (e.g. DTV and set-top boxes), home networking (e.g. xDSL and WiFi), personal entertainment (e.g. digital cameras and portable media players) and microcontrollers (MCUs). MIPS also licenses its 32- and 64-bit architectures to system-on-chip (SoC) developers.

The MIPS32® family of processors is based on a standard, compatible architecture. MIPS32 4K®-based processor cores including the MIPS32 M4K®, 4KE® and 4KSd™ cores are specifically designed to address the requirements of high performance, low power and ease of design for cost-sensitive embedded applications such as MCUs and consumer electronics.

A superset of the popular MIPS32 4KEc® core, the M14Kc core is one of the newest members of the 4KE family, and one of the first MIPS® processors that includes the microMIPS™ code compression Instruction Set Architecture (ISA). microMIPS offers MIPS32 performance with equivalent 16-bit code density. The M14Kc core incorporates design enhancements and application-specific features that are optimized for Linux, Java and Android based digital home equipment.

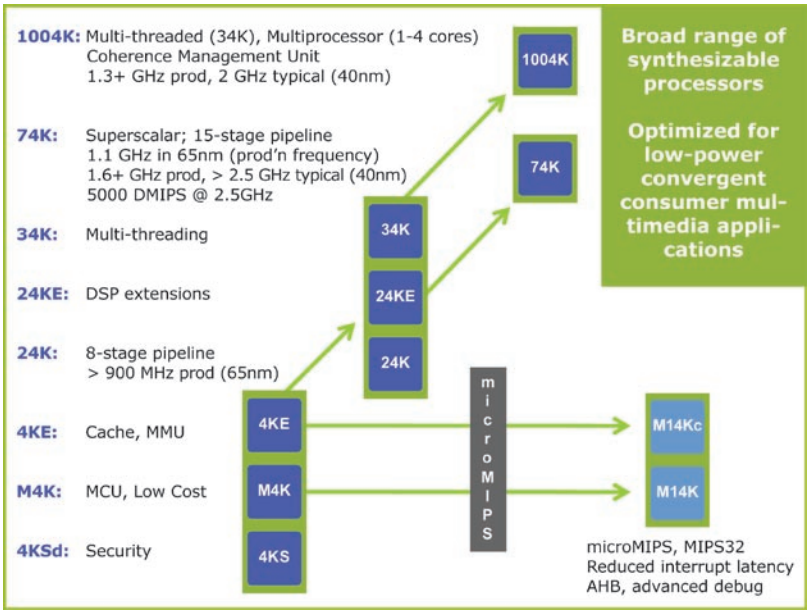

Figure 1: MIPS32 processor core roadmap

1.1 Performance Efficiency

Achieving higher levels of performance is not only a function of increasing the clock frequency, but is also influenced by the instruction per cycle (IPC) efficiency of the execution unit, the depth of the pipeline core and the speed of access to memory-resident code and data.

Performance efficiency is a combination of operating clock frequency and IPC that provides a practical measure of the optimal frequency, power and silicon size that a device will use in executing a specific application.
The M14Kc core can achieve a 300 MHz production frequency @ 90nm, and is based on the established 4K micro-architecture, which includes an execution unit that delivers high performance efficiency of 1.5 DMIPS/MHz.

1.2 Cost Reduction

Minimizing silicon cost without compromising performance or software development capabilities is a key design criteria and competitive differentiator for embedded system developers.

The M14Kc core implements the new microMIPS ISA that can reduce code memory size by 35% compared to MIPS32—leading to a corresponding reduction in silicon size and cost.

A high level of configurability and build-time options designed into the architecture lead to additional cost savings. The synthesizable, scalable M14Kc processor core maintains a high level of performance at lower clock frequencies across a wide range of geometries and standard processes, enabling an additional reduction in silicon size by synthesizing to a smaller, area-optimized configuration.

1.3 Application-Specific Features

A unique combination of intensive signal processing, pervasive use of Linux and increasingly larger and more sophisticated content and application software define and determine the type of features and functions that are required for an effective consumer device and communication-centric system solution.

Media-centric systems, such as those found in the digital home and personal entertainment markets, are required to transfer large blocks of data in a limited amount of time at high clock frequencies. The SoCs typically found in these systems have multimedia and network functionality that is highly interrupt-driven and deterministic in nature, requiring real-time performance with limited bandwidth availability. The M14Kc core provides enhanced interrupt handling capabilities to reduce interrupt latency, hardware multiply/divide and atomic-bit instructions that address this key challenge.

In addition to its high-performance micro engine, the M14Kc core provides an efficient cache controller and Translation Lookaside Buffer Memory Management Unit (TLB MMU) that is mandatory for Linux, Java and Android operations.

A new feature in the M14Kc core is the introduction of an optional AHB-Lite Bus Interface Unit (BIU), enabling easier connectivity to a wide range of peripheral sub-blocks such as USB, Ethernet and media decoders.

1.4 Fast Time to Market

Embedded application controllers, even entry-level low-footprint types, must now incorporate more advanced, complex communications subsystems that are controlled by large amounts of 'threaded' applications software. This makes product debug and development critical in overall project management, and key in determining time to market.

The M14Kc core has an easy-to-program and well-established architecture, supported by a large set of hardware and software development tools that are available from MIPS Technologies and a range of third party vendors.

The M14Kc core includes several on-chip debug and profiling features, available through the industry standard EJTAG port, that enable faster, and more accurate, hardware and software by efficient use of iFlowtrace™, breakpoints, data address sampling, performance counters on multiple event types and 'hot-spot' analysis. All of these are supported within the MIPS System Navigator™ debug probe.

The MIPS-supplied SoC development platform SEAD-3 and a set of cycle accurate and instruction accurate simulators provide additional reductions in development time and cost. These technologies enable designers to develop hardware and software in parallel with a comprehensive and flexible co-simulation environment.

1.5 Expandability

The M14Kc core includes the optional support of Co-Processor2 (CoP2) and CorExtend™ expansion features that are available across the range of MIPS processor cores. The CoP2 interface enables high performance communication with the M14Kc core and customer-specific IP. The CorExtend User Defined Interface (UDI) block enables the implementation of application-specific instructions to be tightly coupled to the processor, extending the capabilities of an M14Kc-based system design.

2. M14Kc Processor Architecture and Features

At the heart of the M14Kc core is a 5-stage pipeline load/store execution unit that is MIPS32 Release 2 Architecture compliant, delivering a Dhrystone performance of 1.5 DMIPS/MHz across the complete operating frequency range.

The central core is a dual-decoder design incorporating the industry-standard MIPS32 instruction decoder and the microMIPS ISA decoder, providing both legacy MIPS32 code support and advanced code compression capability.

The M14Kc core is a superset of the 4KEc processor core, designed from the same 4K micro-architecture. It is enhanced from the 4KEc core with the addition of improved interrupt handling mechanism, reduced interrupt latency, more debug/profiling modes, native AHB-Lite Bus Interface Unit and parity support.

Connection to memory is via a programmable cache controller and optional scratchpad controller. The M14Kc core contains required and optional functional blocks with a high degree of configurability, allowing the design to be more closely aligned with the requirements of the system design.

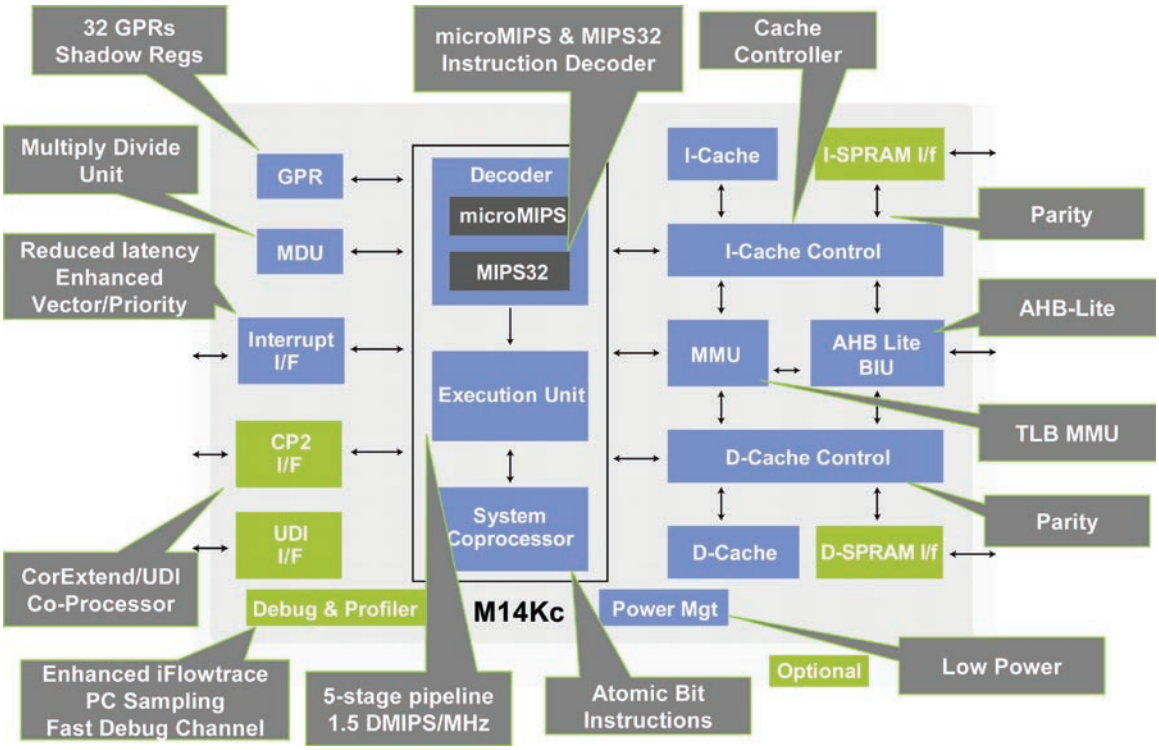

Figure 2: M14Kc core feature block diagram

2.1 Retained Features from the 4KEc

The M14Kc core retains all of the basic features from its predecessor, the 4KEc, including the MIPS32 instruction set decoder/execution unit, cache controller, TLB MMU, general purpose/shadow register sets, vectored interrupt controller and multiply/divide unit (MDU). The M14Kc core maintains full backward-compatibility with the MIPS32 architecture, as well as the 4KEc core pipeline flow and functionality.

The M14Kc core pipeline has 5 stages (see fig 3), with a bypass mechanism that allows the result of an operation to be sent directly to the instruction that needs it without having to perform the register write-read operation, reducing latency and improving IPC. microMIPS instructions are recoded during the I-stage.

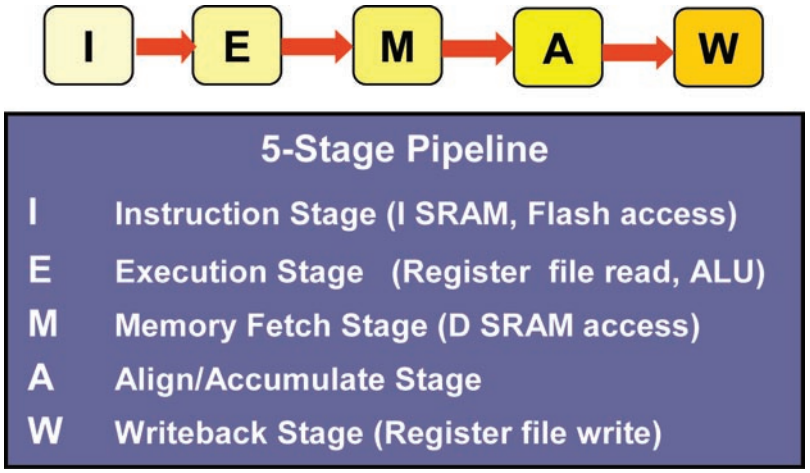

Figure 3: 5-stage pipeline

The M14Kc core contains thirty two 32-bit general purpose registers (GPRs) used for address calculation and integer data manipulation. Additional 32-bit register files, up to 16 sets, are optionally available for use as shadow registers to improve the latency and context switching of interrupt handling routines.

The MDU has its own pipeline that operates in parallel with the core pipeline, which does not cause long operations, such as divide, to stall execution of other system code. The MDU supports execution of 16x16 and 32x16 multiply operation every clock cycle, and 32x32 in 2 clock cycles. 32-bit divide operations complete in 33 cycles. The MDU supports MAC-type instructions commonly used in DSP applications.

The M14Kc core contains a TLB MMU that provides a virtual-to-physical address translation, with selectable attributes, interface between the Execution Unit and cache controller. The cache controller provides a high-performance interface to tightly coupled instruction and data cache memories configurable in size, organization and associativity.

2.2 microMIPS ISA

The M14Kc core is one of the first MIPS processors designed with the microMIPS code compression ISA included in the core design. microMIPS is a complete ISA with a mix of both 16- and 32-bit instructions that supports all MIPS32 instructions, with some of the most commonly used instructions recoded into 16-bit instructions. microMIPS includes 15 new 32-bit instructions and 39 new 16-bit instructions. microMIPS delivers 98% of MIPS32 performance while reducing memory size by 35% versus code containing MIPS32-only instructions.

Figure 4 shows the results of relative Dhrystone performance and code size reduction executing the CSiBE benchmark for MIPS32 and microMIPS.

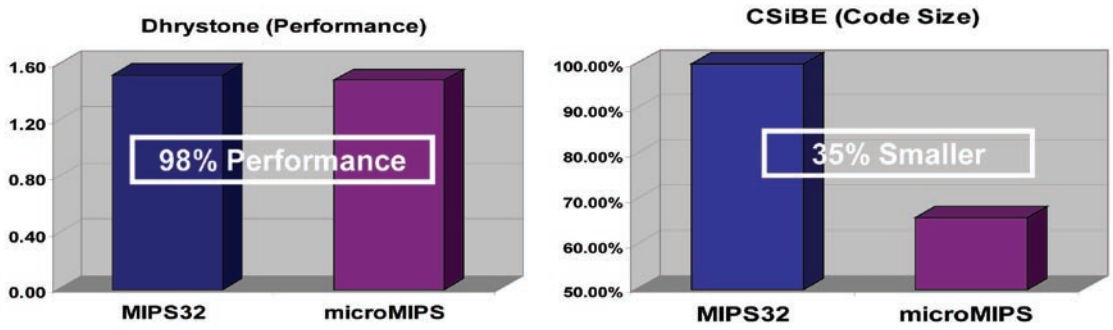

Figure 4: microMIPS performance and code size

The microMIPS instruction decoder fits inside the existing 4K pipeline architecture without affecting compatibility with the microarchitecture. Logic has been implemented to support and control misaligned instructions, improving performance and code density. microMIPS supports co-existence with the legacy MIPS32 decoder, and is assembly level- and ABI- compatible with MIPS32.

Support for microMIPS code development and debug is provided by a complete software toolchain and hardware development platform.

2.3 Interrupt handling

Typical embedded systems have a high number of interrupts, with the majority connected to critical real-time functions that require efficient servicing in a constrained number of clock cycles to enter into and implement the Interrupt Service Routine (ISR).

The M14Kc core has several advanced features in the interrupt handling mechanism that extend the number of serviceable interrupts to 255 from an external controller, and enhanced hardware assist to reduce the vector generation and context switching times.

The M14Kc core implements a new hardware-assisted feature, combined with the use of shadow registers, that reduces interrupt latency (the time from when the interrupt is recognized to the start of ISR execution). This is accomplished through the use of faster

interrupt vector prefetching and dedicated hardware to automatically read and store the core status and GPRs. A similar mechanism is used to unwind the stack and restore the core state when exiting the interrupt service. Interrupt latency is 10 cycles to enter the service routine (Interrupt Prologue) and 4 cycles to exit from the service routine (Interrupt Epilogue).

The M14Kc core also implements interrupt chaining, accelerating the time needed to service multiple valid interrupts that may be pending at the same time. A new instruction (IRET), with the use of dedicated hardware including shadow registers, automates the Interrupt Epilogue and tailchaining process, reducing latency to 4 and 7 cycles respectively.

2.4 Cache Controller

The M14Kc core includes a programmable cache controller that supports individually configured instruction and data caches with sizes expandable up to 64KB. Direct mapped, 2-, 3- or 4- way associativity is supported in write-through and write-back protocols. Each cache has its own 32-bit data path and can be accessed in a single processor cycle. Performance of the cache controller is enhanced by having both the instruction and data caches virtually indexed, enabling the virtual-to-physical translation to occur in parallel with the cache access, removing the delay associated with the address translation.

The M14Kc core supports instruction and data cache locking, enabling critical code or data to be protected and managed more efficiently. The cache controller also has built in support for replacing one-way of the cache with scratchpad memory.

2.5 Memory Management Unit (MMU)

The purpose of an MMU is to translate virtual addresses into a physical memory addresses and to provide protection of code and data that is being used in an application. Running the Linux OS and applications requires that the SoC have an MMU. The M14Kc core contains a highly flexible MMU that can be build-time configured to be of either a TLB or Fixed Mapping Translation (FMT) type.

The TLB MMU can be further configured as either a 4-entry instruction and data or a 16- or 32- dual entry TLB with variable page size capability with programmable read/ write/ execute inhibit page protection attributes. By default, the minimum page size is 4KB, which can be configured at build time to be reduced to 1KB, offering tighter control of the system software.

2.6 Debug and Profiling

An Enhanced JTAG (EJTAG) interface provides the physical access for high-speed debugging and profiling of an M14Kc-based system. The EJTAG interface connects to the Test Access Port (TAP) used for transferring trace and debugs data between the M14Kc core and debug probe.

The M14Kc core provides both simple and complex breakpoint support, configurable to a wide range of instruction and data breakpoint types. Simple/complex I- and D-breakpoints, enhanced iFlowtrace, Fast Debug Channel (FDC), Performance Counters (PCs) and PC data/address sampling functions are additions to the core's existing debug and profiling capabilities.

iFlowtrace is a low-cost, efficient facility that traces the instruction PC. The M14Kc core adds special event and tracing modes to iFlowtrace, extending its usability and effectiveness in accelerating system debug and development. For program analysis, two new sets of Performance Counters can be used to count internal, predefined events, such the number of specific instructions that have been executed in a set time period. Instruction PC and/or load-store addresses can be sampled periodically to provide data for use in 'hot-spot' analysis and program profiling.

The M14Kc core contains an optional Fast Debug Channel (FDC) that provides high bandwidth access to the M14Kc core status with low overhead and interruption to the processor core—in effect, offering a real-time debug capability.

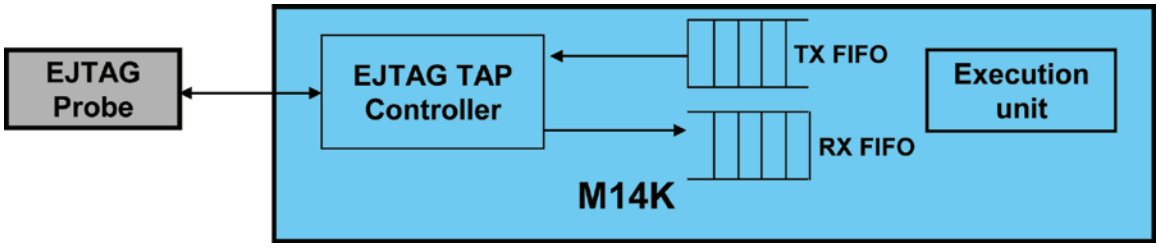

Figure 5: Fast Debug Channel

The FDC incorporates two configurable transmit/receive FIFOs that provide a buffering scheme to serially transfer the M14Kc core data and status information with low processor overhead.

2.6 Configurability

With the M14Kc core, designers can enable or configure a significant number of features at either build time or during run-time, allowing for implementation of an optimized, cost-minimized specific application. Table 1 summarizes the configuration options available.

Feature	Configurability

microMIPS	optional
Shadow register sets	1,2, 4, 8 or 16
MDU	Speed- or area-optimized
I-cache size	0 – 64 KB
I-cache associativity	1, 2, 3 or 4 way
D-cache size	0 – 64 KB
D-cache associativity	1, 2, 3 or 4 way
Parity support	optional
Scratchpad RAM interface	optional
Interrupt vector generation	vector input or 16-bit register
EJTAG	optional
iFlowtrace 2.0	optional
PC sampling	optional
Performance counters	optional
Instruction/Data breakpoints	0/0, 2/1, 4/2, 6/2, 8/4
FDC FIFO	2 Tx/2 Rx, 8 Tx/4 Rx
Power management	clock gating, WAIT instruction
CoProcessor 2	optional
CorExtend/UDI	optional

Table 1: Configurability options

3.0 Summary

The new M14Kc core is one of the first MIPS processors designed with the new microMIPS ISA, resulting in an enhanced high-performance, low area/cost, and low-power MIPS32-compatble core successor to the 4KEc core.

The M14Kc core is supported by a comprehensive, integrated set of software and hardware development tools, a new evaluation/development platform and a broad ecosystem of third party partners.

With a high-performance and efficient 1.5DMIPS/MHz microarchitecture and advanced code compression capability from microMIPS, along with new and enhanced application-specific features, the M14Kc core an ideal solution for cost-sensitive, low footprint embedded applications in the digital home, personal entertainment and networking markets.

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